WT56F116S/108S
3T 8052 Micro-controller with ADC + DAC + LCD Driver (FLASH)

Data Sheet

Rev. 1.0

May 2017

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Table of Contents

1. General Description

The WT56F116S/108S is a general-purpose single chip Microcontroller with LCD function. In addition to using the advanced 3T 8052 single-chip core, wide and low operating voltage range (1.8V ~ 3.6V), and high noise immunity, the product consists of 16Kx8/8Kx8 Flash Program Memory, 768x8 RAM, abundant peripheral resources and versatile power management (refer to the content for more details).

The above features make the WT56F116S/108S suitable for a wide range of applications, especially in areas such as Sensor Hub, Signal Conditioner, Voice Recorder/Player, and so on. The WT56F116S/108S is a low cost high performance product with kinds of package to replace the mainstream products on the market. In order to contribute more competitive ability, Weltrend also provides dice and wafer sale for the customer.

Part No.	Core	PROM (Byte)	SRAM (Byte)	I/O (Max)	LCD (CxS)	PWM	ADC	DAC	Interface	LDO18 Capacitor	PKG Type
WT56F108	3T-8052	8K	384	56	4x40	16-bitx2	10-bitx16	X	UARTx1	X	64/44 LQFP 28SOP
WT56F108S	3T-8052	8K	768	45	4x32	16-bitx2	10-bitx16	10-bitx1	I^2C(M/S) x 2 UART x 2 SPI x 1	need	64/48 LQFP 28SOP 20SSOP
WT56F116S	3T-8052	16K	768	45	4x32	16-bitx2	10-bitx16	10-bitx1	I^2C(M/S) x 2 UART x 2 SPI x 1	need	64/48 LQFP 28SOP 20SSOP

2. Features

WT56F116S/108S is an advanced 8052 Micro-controller with LCD Driver, and it also provides the following features.

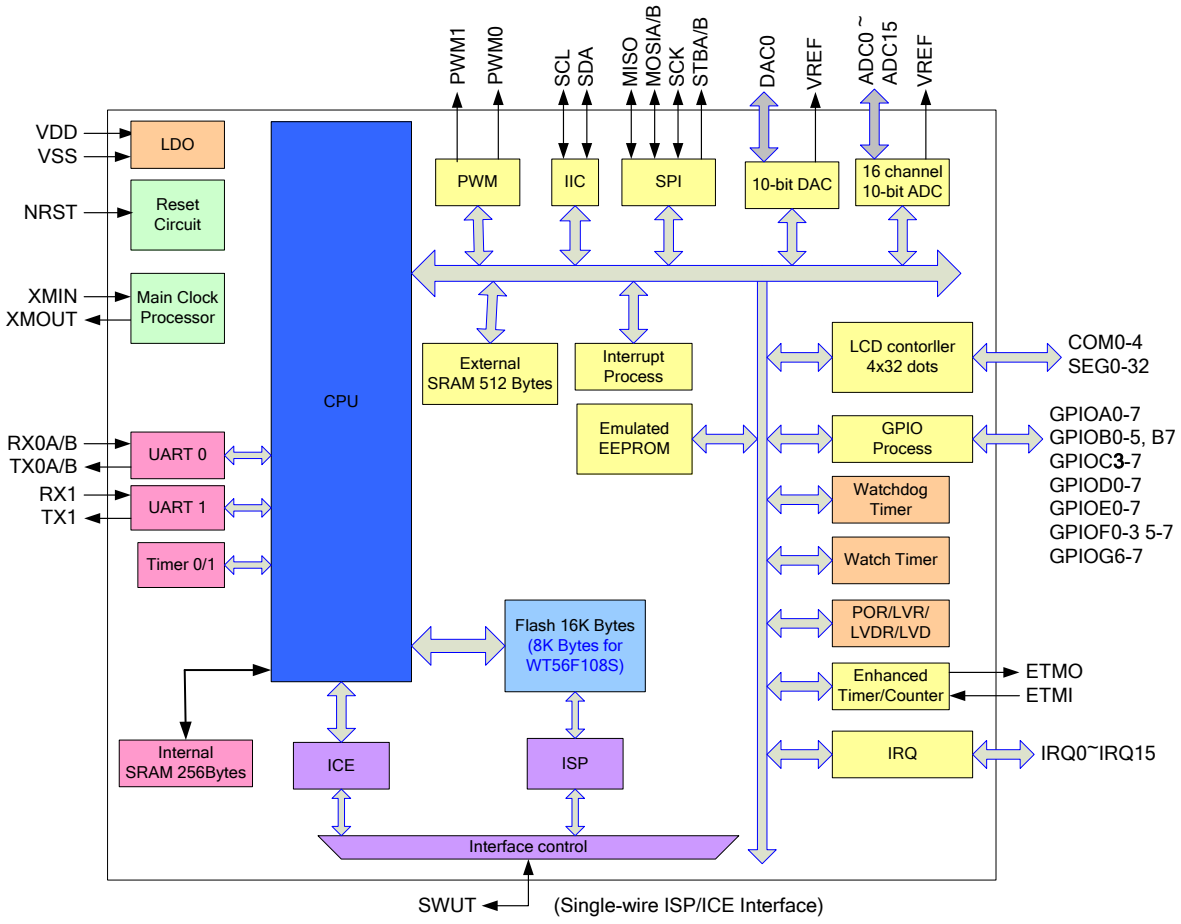
- 3T 8052 core, MCS-51 instruction set compatible
- Instruction execution time: Min. = 125ns @24 MHz
- 768 Bytes of RAM (256 Bytes of standard 8052 internal Data RAM and 512 Bytes of external RAM)
- 16K Bytes of flash memory for program storage
- Supporting Internal & External Clock Oscillators:
  - Internal clock: 12/24 MHz RC oscillator & 32 kHz RC oscillator
  - External clock: External DC ~ 24 MHz Crystal Oscillator
- Two 16-bit Timer/Counters (Timer0 & Timer1)
- One Watchdog Timer (WDT)
- One Watch Timer
- One 16-bit Enhanced Timer with Capture function
- Two UARTs (UART0 & UART1), support baud rate 1200 bps ~ 230400 bps (at 12 MHz)
- Emulated E^2PROM
- One master/slave SPI interface
- Two master/slave I^2C interface
- Two 16-bit PWMs (PWM0 & PWM1)
- LCD Control Driver
  - 4 COM x 32 SEG
- 16-channel 10-bit Analog/Digital Converter (ADC0 ~ ADC15)
- 1-channel 10-bit Digital/Analog Converter (DAC0)
- Three power-saving modes: Sleep mode, Green mode and Idle mode
- 8 external Interrupt IRQ pins (IRQ0 ~ IRQ7)
- 45 programmable bi-directional I/O pins, 12 of them with both high current sink/source ability (10 mA)

- Programmable Low Voltage Detection Reset (LVDR)
- On-chip Power On Reset (POR) and Low Voltage Reset (LVR)
- Built-in single-wire In-Circuit Emulator (ICE) and In-System Programming (ISP)
- Read Out Protection
- Operating voltage range: 1.8V ~ 5.5V
- Operating temperature: -40℃ ~ +105℃
- Package (Green Package): LQFP64, LQFP48, SOP28 & SSOP20

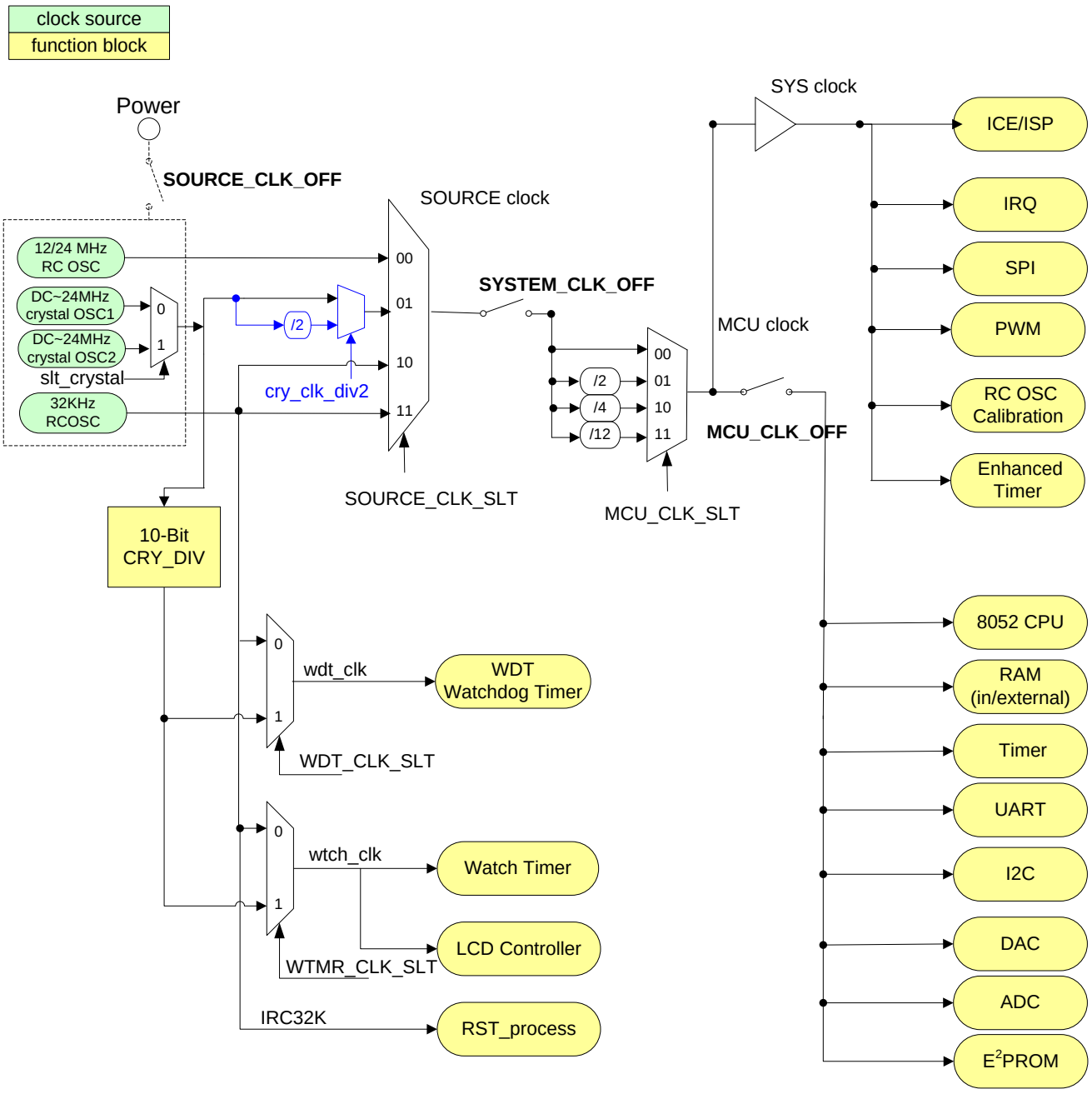
For more details about WT56F116S/108S power consumption (@3V) in different operation modes, please refer to Section 6.7 Power Management.

- ✓ If you want to use the UART must consider if IRC 12 MHz frequency offset is greater than ±3%, must use the external LDO regulator if necessary
- ✓ This product provides external 32768 Hz crystal oscillator to calibrate IRC 12 MHz automatically and keeps the frequency tolerance < ±1%

3. Block Diagram



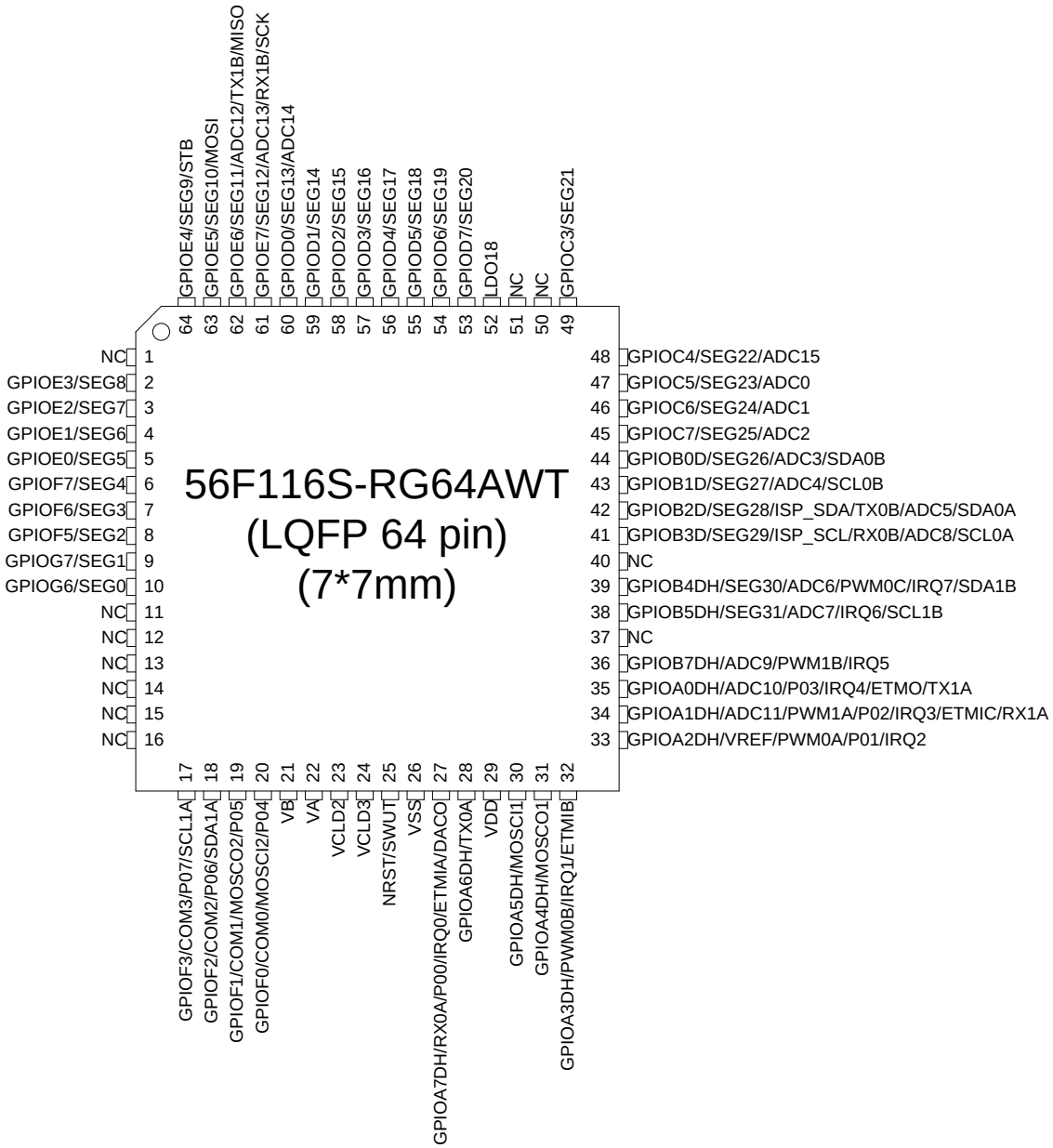
3.1 System Clock Tree



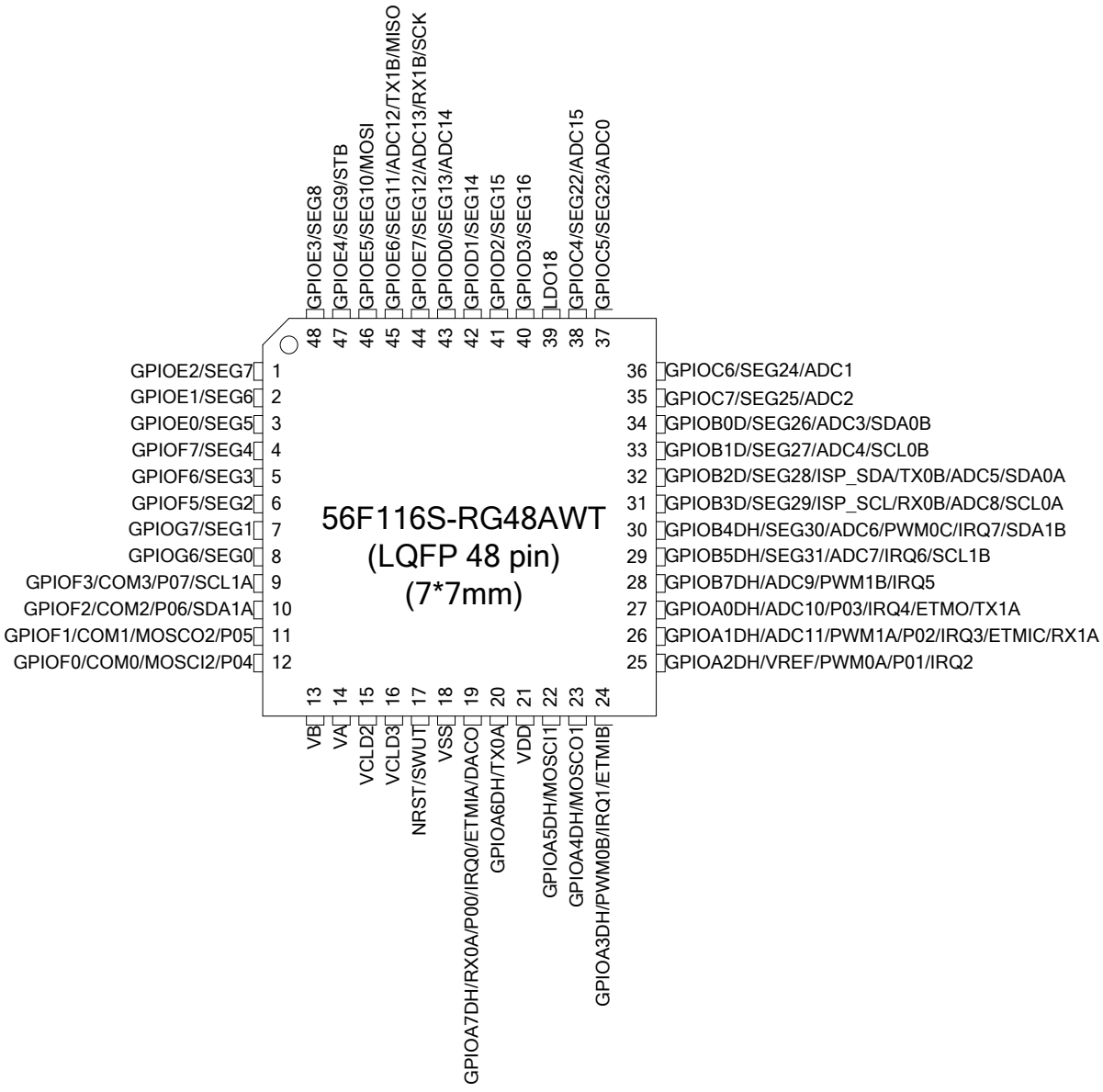
* When using the external Crystal Oscillator, please select the corresponding driving ability according to its frequency. Refer to Oscillator Driver Control Register (XFR: 0x08) CRY_12M_DR[2:0] bit for more details.

4. Pin Configuration

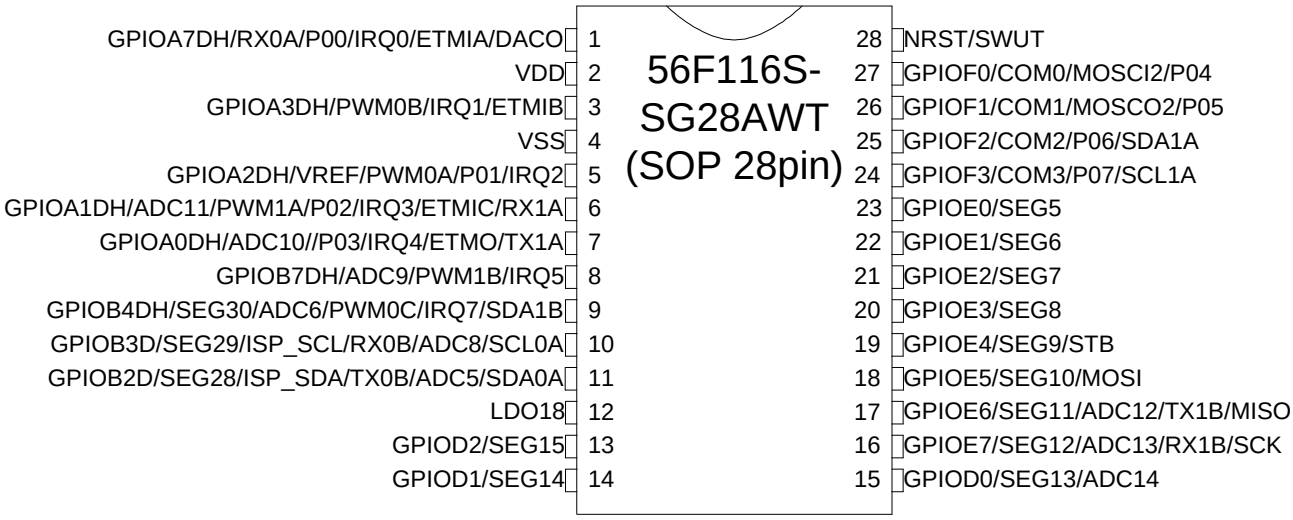
WT56F116S-RG64AWT 64-Pin LQFP (same as WT56F108S)



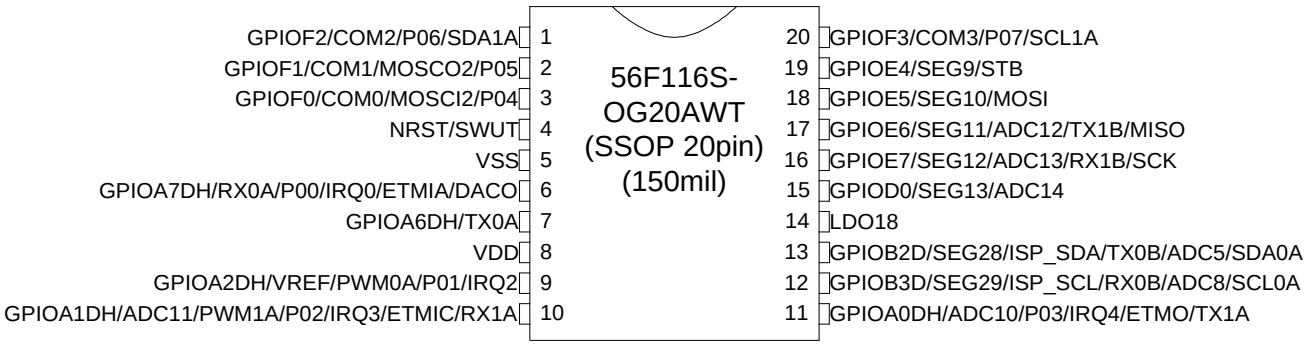
WT56F116S-RG48AWT 48-Pin LQFP (same as WT56F108S)



WT56F116S-SG28AWT 28-Pin SOP (same as WT56F108S)



WT56F116S-OG20AWT 20-Pin SSOP (same as WT56F108S)



4.1 Pin Description

Pin Number				Pin Name		Primary Functions	
RG64A WT	RG48A WT	SG28A WT	OG20A WT		I/O	Descriptions	Circuit Type
1						NC	
2	48	20		GPIOE3/ SEG8	I/O	GPIOE3: General-purpose I/O with push-pull SEG8: LCD segment 8	E4
3	1	21		GPIOE2/ SEG7	I/O	GPIOE2: General-purpose I/O with push-pull SEG7: LCD segment 7	E4
4	2	22		GPIOE1/ SEG6	I/O	GPIOE1: General-purpose I/O with push-pull SEG6: LCD segment 6	E4
5	3	23		GPIOE0/ SEG5	I/O	GPIOE0: General-purpose I/O with push-pull SEG5: LCD segment 5	E4
6	4			GPIOF7/ SEG4	I/O	GPIOF7: General-purpose I/O with push-pull SEG4: LCD segment 4	E4
7	5			GPIOF6/ SEG3	I/O	GPIOF6: General-purpose I/O with push-pull SEG3: LCD segment 3	E4
8	6			GPIOF5/ SEG2	I/O	GPIOF5: General-purpose I/O with push-pull SEG2: LCD segment 2	E4
9	7			GPIOG7/ SEG1	I/O	GPIOG7: General-purpose I/O with push-pull SEG1: LCD segment 1	E4
10	8			GPIOG6/ SEG0	I/O	GPIOG6: General-purpose I/O with push-pull SEG0: LCD segment 0	E4
11						NC	
12						NC	
13						NC	
14						NC	
15						NC	
16						NC	
17	9	24	20	GPIOF3/ COM3/ P07/ SCL1A	I/O	GPIOF3: General-purpose I/O with push-pull COM3: LCD common 3 P07: 8051 P0.7 SCL1A: 1st IIC SCL path A	E4
18	10	25	1	GPIOF2/ COM2/ P06/ SDA1A	I/O	GPIOF2: General-purpose I/O with push-pull COM2: LCD common 2 P06: 8051 P0.6 SDA1A: 1st IIC SDA path A	E4
19	11	26	2	GPIOF1/ COM1/ MOSCO2/ P05	I/O	GPIOF1: General-purpose I/O with push-pull COM1: LCD common 1 MOSCO2: the crystal output pin of path 2 P05: 8051 P0.5	B3
20	12	27	3	GPIOF0/ COM0/ MOSCI2/ P04	I/O	GPIOF0: General-purpose I/O with push-pull COM0: LCD common 0 MOSCI2: the crystal oscillator input pin of path 2 P04: 8051 P0.4	B3
21	13			VB	O	Connect the LCD capacitors B	
22	14			VA	O	Connect the LCD capacitors A	

Pin Number				Pin Name		Primary Functions	
RG64A WT	RG48A WT	SG28A WT	OG20A WT		I/O	Descriptions	Circuit Type
23	15			VLCD2	O	2/3 bias voltage	
24	16			VLCD3	O	1/3(1/2) bias voltage	
25	17	28	4	NRST/ SWUT	I	NRST: reset pin SWUT: single-wire ISP/ICE interface	D
26	18		5	VSS	GND	Core ground	
27	19	1	6	GPIOA7DH/ RX0A/ P00/ IRQ0/ ETMIA/ DACO	I/O	GPIOA7DH: General-purpose I/O with programmable high current sink/source push-pull or open drain RXA: Receive data input of path A of UART P00: Mapping to 8052 P0.0 IRQ0: External Interrupt Request 0 ETMIA: Enhanced Timer/Counter clock source capture input of path A DACO: DAC output	A
28	20		7	GPIOA6DH/ TX0A	I/O	GPIOA6DH: General-purpose I/O with programmable high current sink/source push-pull or open drain TXA: Transmit data output of path A of UART	A
29	21	2	8	VDD	PWR	VDD power: external 4.7uf + 0.1uF	
30	22			GPIOA5DH/ MOSCI1	I/O	GPIOA5DH: General-purpose I/O with programmable high current sink/source push-pull or open drain MOSCI1: the crystal oscillator input pin of path 1	B1
31	23			GPIOA4DH/ MOSCO1	I/O	GPIOA4DH: General-purpose I/O with programmable high current sink/source push-pull or open drain MOSC01: the crystal oscillator output pin of path 1	B1
32	24	3		GPIOA3DH/ PWM0B/ IRQ1/ ETMIB	I/O	GPIOA3DH: General-purpose I/O with programmable high current sink/source push-pull or open drain PWM0B: PWM0 output pin of path B IRQ1: External Interrupt Request 1 ETMIB: Enhanced Timer/Counter clock source capture input of path B	A
		4		VSS	GND	Core ground	
33	25	5	9	GPIOA2DH/ VREF/ PWM0A/ P01/ IRQ2	I/O	GPIOA2DH: General-purpose I/O with programmable high current sink/source push-pull or open drain VREF: Analog/Digital Converter Voltage Reference Input pin PWM0A: PWM0 output pin of path A P01: Mapping to 8052 P0.1 IRQ2: External Interrupt Request 2	E2

Pin Number				Pin Name		Primary Functions	
RG64A WT	RG48A WT	SG28A WT	OG20A WT		I/O	Descriptions	Circuit Type
34	26	6	10	GPIOA1DH/ ADC11/ PWM1A/ P02/ IRQ3/ ETMIC/ RX1A	I/O	GPIOA1DH: General-purpose I/O with programmable high current sink/source push-pull or open drain ADC11: Analog/Digital Converter Input 11 PWM1A: PWM1 output pin of Path A P02: Mapping to 8052 P0.2 IRQ3: External Interrupt Request 3 ETMIC: Enhanced Timer/Counter clock source capture input of path C RX1A: UART1 receive path A	C1
35	27	7	11	GPIOA0DH/ ADC10/ P03/ IRQ4/ ETMO/ TX1A	I/O	GPIOA0DH: General-purpose I/O with programmable high current sink/source push-pull or open drain ADC10: Analog/Digital Converter Input 10 P03: Mapping to 8052 P0.3 IRQ4: External Interrupt Request 4 ETMO: Compare Result Output of Enhanced Timer/Counter TX1A: UART1 transmit path A	C1
36	28	8		GPIOB7DH/ ADC9/ PWM1B/ IRQ5	I/O	GPIOB7DH: General-purpose I/O with programmable high current sink/source push-pull or open drain ADC9: Analog/Digital Converter Input 9 PWM1B: PWM1 output pin of path B IRQ5: External Interrupt Request 5	C1
37						NC	C1
38	29			GPIOB5DH/ SEG31/ ADC7/ IRQ6/ SCL1B	I/O	GPIOB5DH: General-purpose I/O with programmable high current sink/source push-pull or open drain SEG31: LCD segment 31 ADC7: Analog/Digital Converter Input 7 IRQ6: External Interrupt Request 6 SCL1B: 1st IIC SCL path B	C1
39	30	9		GPIOB4DH/ SEG30/ ADC6/ PWM0C/ IRQ7/ SDA1B	I/O	GPIOB4DH: General-purpose I/O with programmable high current sink/source push-pull or open drain ADC6: Analog/Digital Converter Input 6 PWM0C: PWM0 output pin of path C IRQ7: External Interrupt Request 7 SDA1B: 1st IIC SDA path B	C1
40						NC	
41	31	10	12	GPIOB3D/ SEG29/ ISP_SCL/ RX0B/ ADC8/ SCL0A	I/O	GPIOB3: General-purpose I/O with programmable open drain SEG29: LCD segment 29 ISP_SCL: ISP I^2C SCL RXB: Receive data input of path B of UART ADC8: Analog/Digital Converter Input 8 SCL0A: 0th IIC SCL path A	E6

Pin Number				Pin Name		Primary Functions	
RG64A WT	RG48A WT	SG28A WT	OG20A WT		I/O	Descriptions	Circuit Type
42	32	11	13	GPIOB2D/ SEG28/ ISP_SDA/ TX0B/ ADC5/ SDA0A	I/O	GPIOB2D: General-purpose I/O with programmable open drain SEG28: LCD segment 28 ISP_SDA: ISP I^2C SDA TX0B: Transmit data output of path B of UART ADC5: Analog/Digital Converter Input 5 SDA0A: I^2C SDA 0^{th} tunnel A	E6
43	33			GPIOB1D/ SEG27/ ADC4/ SCL0B	I/O	GPIOB1: General-purpose I/O with programmable open drain SEG27: LCD segment 27 ADC4: Analog/Digital Converter Input 4 SCL0B: 0^{th} IIC SCL path B	E6
44	34			GPIOB0D/ SEG26/ ADC3/ SDA0B	I/O	GPIOB0: General-purpose I/O with programmable open drain SEG26: LCD segment 26 ADC3: Analog/Digital Converter Input 3 SDA0B:1^{st} IIC SCL path B	E6
45	35			GPIOC7/ SEG25/ ADC2	I/O	GPIOC7: General-purpose I/O with push-pull SEG25: LCD segment 25 ADC2: Analog/Digital Converter Input 2	E5
46	36			GPIOC6/ SEG24/ ADC1	I/O	GPIOC6: General-purpose I/O with push-pull SEG24: LCD segment 24 ADC1: Analog/Digital Converter Input 1	E5
47	37			GPIOC5/ SEG23/ ADC0	I/O	GPIOC5: General-purpose I/O with push-pull SEG23: LCD segment 23 ADC0: Analog/Digital Converter Input 0	E5
48	38			GPIOC4/ SEG22 ADC15	I/O	GPIOC4: General-purpose I/O with push-pull SEG22: LCD segment 22 ADC15: Analog/Digital Converter Input 15	E4
49				GPIOC3/ SEG21	I/O	GPIOC3: General-purpose I/O with push-pull SEG21: LCD segment 21	E4
50						NC	
51						NC	
52	39	12	14	LDO18	O	LDO18: external 4.7uF + 0.1uF	
53				GPIOD7/ SEG20	I/O	GPIOD7: General-purpose I/O with push-pull SEG20: LCD segment 20	E4
54				GPIOD6/ SEG19	I/O	GPIOD6: General-purpose I/O with push-pull SEG19: LCD segment 19	E4
55				GPIOD5/ SEG18	I/O	GPIOD5: General-purpose I/O with push-pull SEG18: LCD segment 18	E4
56				GPIOD4/ SEG17	I/O	GPIOD4: General-purpose I/O with push-pull SEG17: LCD segment 17	E4
57	40			GPIOD3/ SEG16	I/O	GPIOD3: General-purpose I/O with push-pull SEG16: LCD segment 16	E4
58	41	13		GPIOD2 SEG15	I/O	GPIOD2: General-purpose I/O with push-pull SEG15: LCD segment 15	E4
59	42	14		GPIOD1/ SEG14	I/O	GPIOD1: General-purpose I/O with push-pull SEG14: LCD segment 14	E4

Pin Number				Pin Name		Primary Functions	
RG64A WT	RG48A WT	SG28A WT	OG20A WT		I/O	Descriptions	Circuit Type
60	43	15	15	GPIOD0/ SEG13/ ADC14	I/O	GPIOD0: General-purpose I/O with push-pull SEG13: LCD segment 13 ADC14: Analog/Digital Converter Input 14	E4
61	44	16	16	GPIOE7/ SEG12/ ADC13/ RX1B/ SCK	I/O	GPIOE7: General-purpose I/O with push-pull SEG12: LCD segment 12 ADC13: Analog/Digital Converter Input 13 RX1B: UART1 receive path B SCK: SCK pin of SPI	E4
62	45	17	17	GPIOE6/ SEG11/ ADC12/ TX1B/ MISO	I/O	GPIOE6: General-purpose I/O with push-pull SEG11: LCD segment 11 ADC12: Analog/Digital Converter Input 12 TX1B: UART1 transmit path B MISO: MISO pin of SPI	E4
63	46	18	18	GPIOE5/ SEG10/ MOSI	I/O	GPIOE5: General-purpose I/O with push-pull SEG10: LCD segment 10 MOSI: MOSI pin of SPI	E4
64	47	19	19	GPIOE4/ SEG9/ STB	I/O	GPIOE4: General-purpose I/O with push-pull SEG9: LCD segment 9 STB: STB pin of SPI	E4

Note: All I/O pins are floating on Reset status.

4.2 Pin Summary

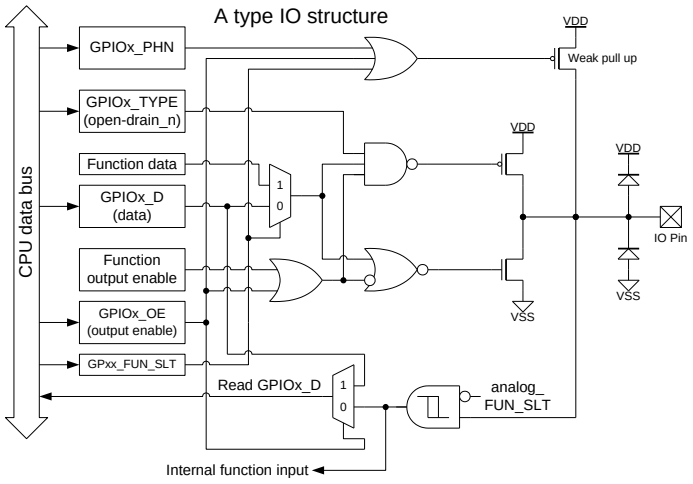
Explain each pin function in details.

Pin Name	Type	Description
PORT		
GPIOA0 ~ GPIOA7	I/O	Bidirectional general-purpose I/O port
GPIOB0 ~ GPIOB7	I/O	Bidirectional general-purpose I/O port **(GPIOB6 not included)**
GPIOC3 ~ GPIOC7	I/O	Bidirectional general-purpose I/O port
GPIOD0 ~ GPIOD7	I/O	Bidirectional general-purpose I/O port
GPIOE0 ~ GPIOE7	I/O	Bidirectional general-purpose I/O port
GPIOF0 ~ GPIOF7	I/O	Bidirectional general-purpose I/O port **(GPIOF4 not included)**
GPIOG6 ~ GPIOG7	I/O	Bidirectional general-purpose I/O port
8052 Port		
P00~P07	I/O	Mapping to 8052 P0.0~P0.7
Enhanced Timer/Counter		
ETMO	O	Enhanced Timer/Counter Compare Result Output
ETMI A/B/C	I	Enhanced Timer/Counter Clock Source or Capture Input of path A, path B or path C
IRQ		
IRQ0 ~ IRQ7	I	8 External Interrupt Request Input pins
PWM		
PWM0 A/B/C	O	PWM 0 Output path A, path B or path C
PWM1 A/B	O	PWM 1 Output path A or path B
UART		
RX 0/1/A/B	I	UART Receive path A or path B of 0^{TH} or 1^{st} group
TX 0/1/A/B	O	UART Transmit path A or path B of 0^{TH} or 1^{st} group
ADC		
ADC0 ~ ADC15	I	16 Analog/Digital Input pins
VREF	I	Analog/Digital converter reference voltage input pins
LCD		
SEG0 ~ SEG31	O	SEGMENT of LCD driver
COM0 ~ COM3	O	COM of LCD driver
VA, VB	O	Connect the LCD capacitors A, B
VLCD2, VLCD3	O	Bias voltage
VCC & VSS		
VDD	PWR	Power
VSS	GND	Ground

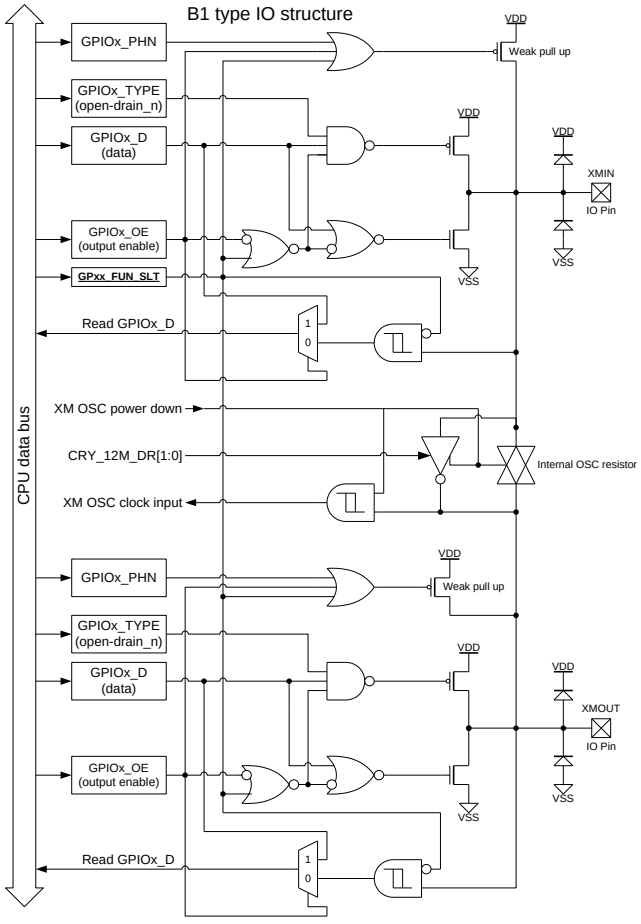
Pin Name	Type	Description
DAC		
DAC0	O	1 Digital/Analog Input pin
SPI		
SCK	I/O	SPI interface clock
MOSI	I/O	SPI Data pin MOSI (Master Output; Slave Input)
STB	O	SPI enable
MISO	I/O	SPI Data pin MISO (Master Input; Slave Output)
I²C		
SCL 0/1/A/B	I/O	0^{th} or 1^{st} path A or B of I²C interface clock
SDA 0/1/A/B	I/O	0^{th} or 1^{st} path A or B of I²C interface data
OSC		
MOSCO 1/2	O	Main crystal oscillator output of path 1 or path 2
MOSCI 1/2	I	Main crystal oscillator input of path 1 or path 2
RESET		
NRST	I	CPU reset
ISP & ICE		
SWUT	I/O	Single-wire ISP & ICE interface

4.3 Port Structure

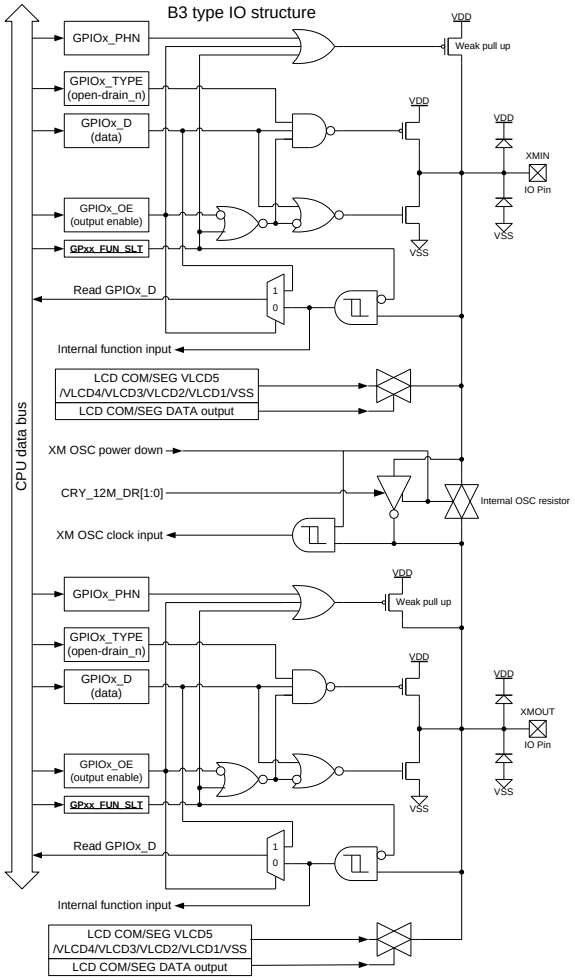
I/O Structure (Type A)



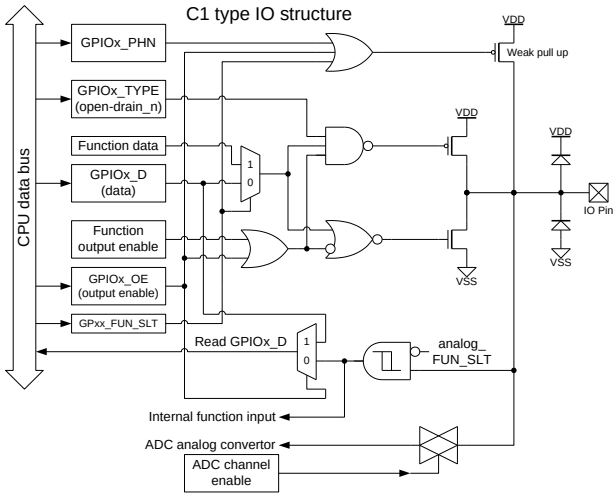
I/O Structure (Type B1)



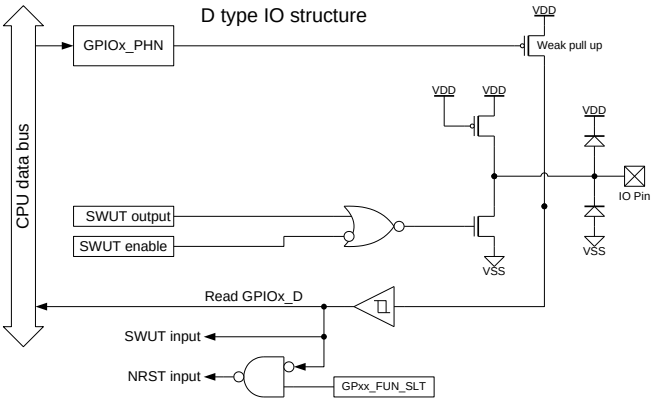
I/O Structure (Type B3)



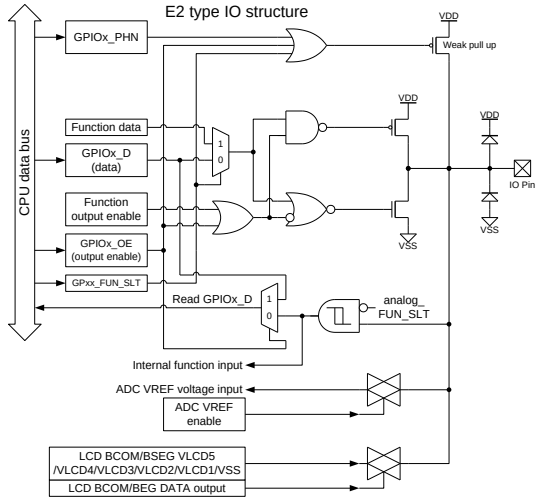
I/O Structure (Type C1)



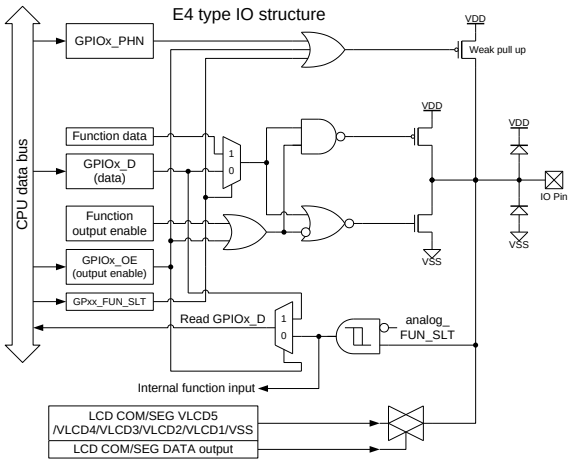
I/O Structure (Type D)



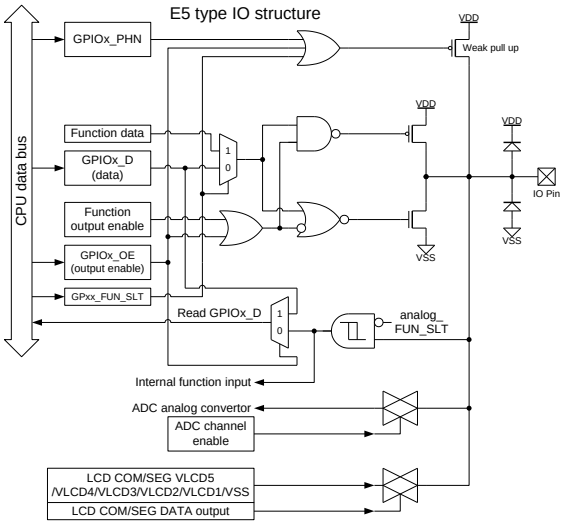
I/O Structure (Type E2)



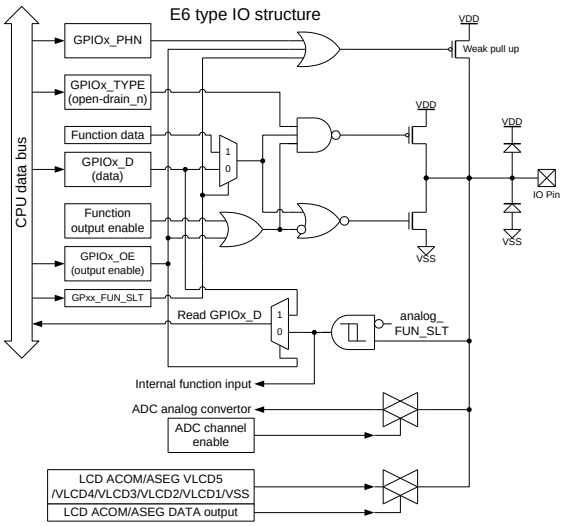
I/O Structure (Type E4)



I/O Structure (Type E5)



I/O Structure (Type E6)



5. Normal Function

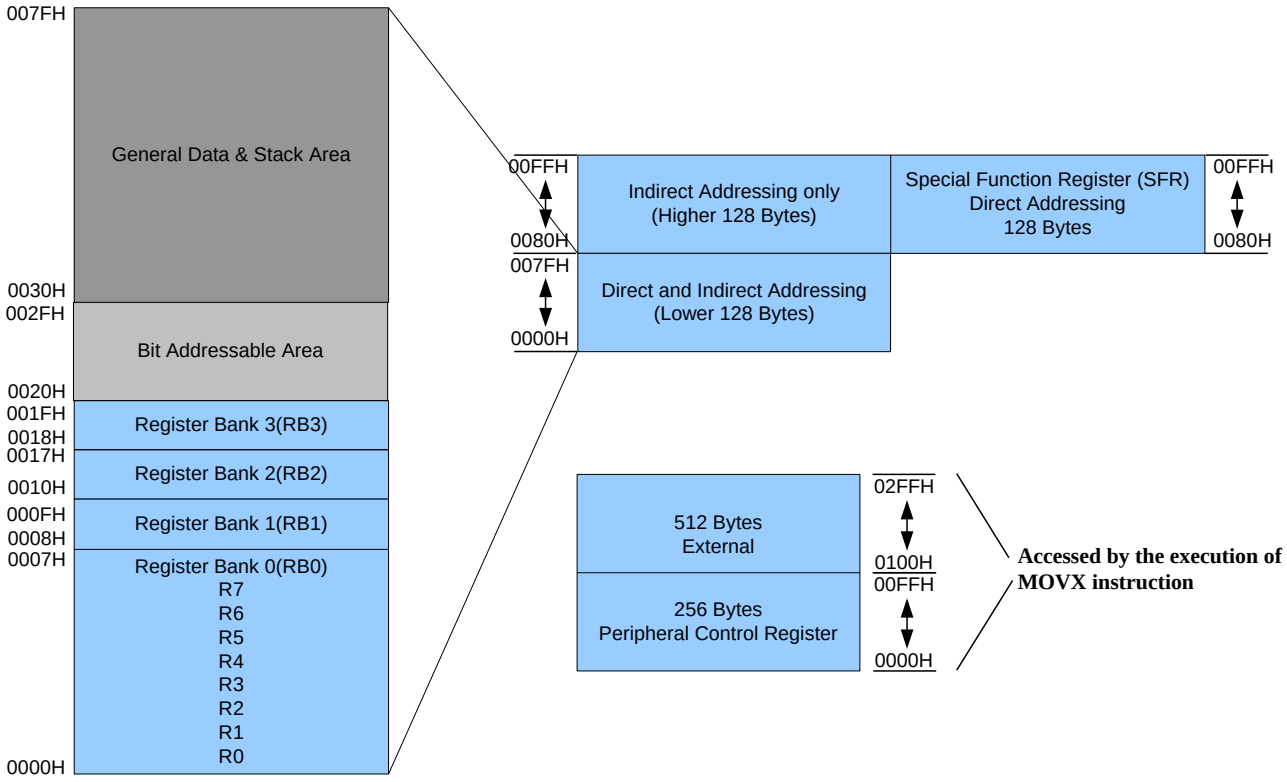
5.1 CPU

The WT56F116S/108S has an embedded 8-bit 3T 8052 compatible CPU with 16-bit space addressable and 8-bit data access functions. The instruction execution time of 3T 8052 is four times faster than that of the conventional 12T 8052. All of the functions and Special Function Register (SFR) definitions will be described in below sections.

5.2 RAM

The WT56F116S/108S consists of 256+512 Bytes of SRAM. The 256 Bytes of RAM is the internal RAM of the general 8052. External 512 Bytes of SRAM can be accessed by the execution of MOVX instruction.

Below figure shows a map of the RAM. For Peripheral Control Registers, see section 6.1.



The internal SRAM contains:
128 Bytes of internal SRAM, locates from 0x0000H to 0x007FH (direct and indirect addressing is allowed)
128 Bytes of internal SRAM, locates from 0x0080H to 0x00FFH (indirect addressing)
512 Bytes of external SRAM, locates from 0x0100H to 0x02FFH (accessed by MOVX instruction)
Its main purpose is for storing data in the program, and therefore it is also called Data Memory. The Data memory of WT56F116S/108S includes the following sections:

(1) The lower 128 bytes of internal SRAM (0000H ~ 007FH) which can be accessed by direct or indirect addressing are divided into three segments:

- **General Purpose Register**: Locates from 0000H to 001FH, 32 Bytes in total, can be divided into four register banks. Each register bank contains eight general-purpose registers (R0~R7). Four

register banks can be selected by the select bit RS1 and RS0 in the Program Status Word Register.

- **Bit Addressable Area**: Locates from 20H to 2FH, 16 Bytes in total. Each one of the 128 bits of this segment can be directly addressed by Bit Addressing.
- **General Data Area:** Locates from 0030H to 007FH, 80 Bytes are available to the user as data RAM (including the Stack area).

(2) The higher 128 bytes of internal SRAM (0080H ~ 00FFH) can be accessed by indirect addressing through R0 or R1 (*).

(3) Special Function Registers (SFR), locates from 0080H to 00FFH, can be accessed by direct addressing (*).

(4) 512 Bytes of external SRAM, locates from 0100H to 02FFH, can be accessed by instruction MOVX.

(*) Although the SFR and the higher 128 Bytes of internal RAM occupy the same addresses (0080H ~ 00FFH), they are two separate areas. MCU will automatically determine which area is in use by two different accessing ways.

5.3 Flash Memory

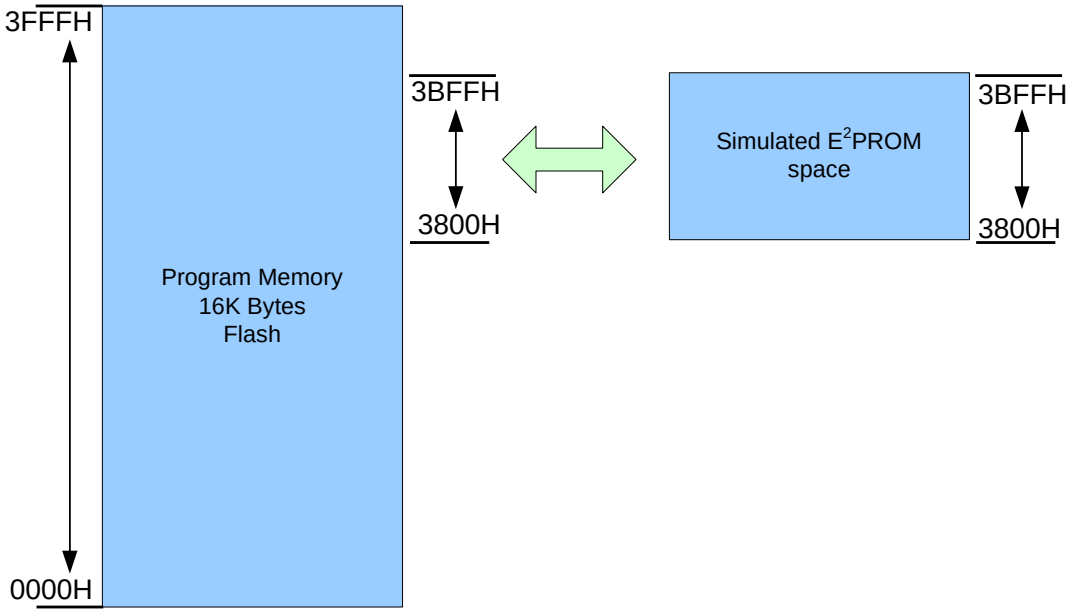
The WT56F116S consists of 16K built-in flash, which can be served as general Program memory or simulated E^2PROM (0x3800H ~ 0x3BFFH);

The WT56F108S consists of 8K built-in flash, which can be served as general Program memory or simulated E^2PROM (0x1800H ~ 0x1BFFH)

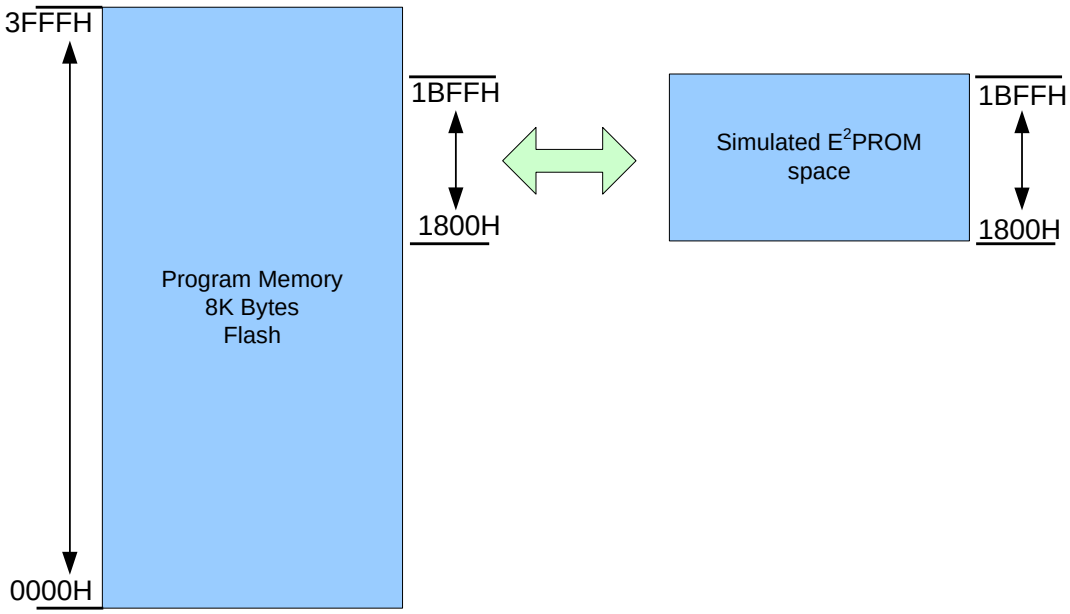
Features as below:

- FLASH memory: 16K Bytes
- Operating voltage: 1.8V ~ 5.5V
- In-System Programming (ISP)
- Over 10 years Data Retention
- Read Out Protection
- Emulated E^2PROM function @1.8V~5.5V

WT56F116S Flash Memory



WT56F108S Flash Memory



Note: The last 8 bytes of FLASH is Code Option, and the available flash ranges from 0x0000H to 0x3FF7H.

5.4 Memory Mapping

WT56F116S/108S built-in 128 Bytes of direct addressing 8052 standard Special Function Register (SFR), as described below.

- CPU Core Register: ACC, B, PSW, SP, DPL0, DPH0
- Interrupt Register: IP, IE, XICON
- I/O port Register: P0
- Timer Register: TCON, TMOD, TL0, TH0, TL1, TH1, CKCON
- UART0 Register: SCON0, SBUF0, SBRG0H, SBRG0L, PCON

Special Function Register (SFR) MAP:

	Bit Addressable	No Bit Addressable							
F8H									FFH
F0H	B								F7H
E8H									EFH
E0H	ACC								E7H
D8H									DFH
D0H	PSW								D7H
C8H									CFH
C0H	XICON								C7H
B8H	IP								BFH
B0H									B7H
A8H	IE								AFH
A0H									A7H
98H	SCON0	SBUF0	SBRG0H	SBRG0L					9FH
90H									97H
88H	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON		8FH
80H	P0	SP	DPL0	DPH0				PCON	87H

Special Function Register (SFR) Table:

Register Name	Address	Reset Value	Description
P0	80H	FFh	Port 0
SP	81H	07h	Stack Pointer
DPL0	82H	00h	Data Pointer 0 low byte
DPH0	83H	00h	Data Pointer 0 high byte
PCON	87H	00h	Power Control Register
TCON	88H	00h	Timer 0/1 Counter Control
TMOD	89H	00h	Timer 0/1 Mode Control
TL0	8AH	00h	Timer 0, low byte
TL1	8BH	00h	Timer 1, low byte
TH0	8CH	00h	Timer 0, high byte
TH1	8DH	00h	Timer 1, high byte
CKCON	8EH	00h	Timer clock-base select

Register Name	Address	Reset Value	Description
SCON0	98H	00h	Serial Port 0, Control Register
SBUF0	99H	00h	Serial Port 0, Data Buffer
SBRG0H	9AH	00h	Serial Baud rate Generator, high byte
SBRG0L	9BH	00h	Serial Baud rate Generator, low byte
IE	A8H	00h	Interrupt Enable Register
IP	B8H	00h	Interrupt Priority Register 1
XICON	C0H	00h	Interrupt Enable Register (INT3)
PSW	D0H	00h	Program Status Word
ACC	E0H	00h	Accumulator
B	F0H	00h	B Register

Note: Refer to 5.7 "Reset" section for the initial value of SFR.

Introduction of WT56F116S/108S CPU SFR is as below:

B: Address: F0H **Reset Value: 00h**

7	6	5	4	3	2	1	0
B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0

The B register is used during multiply and divide operations. It can store the multiplier and the high bytes of operation result in multiply operation, and also the divisor and the remainder of operation result in divide operation. The B register can be used as a general register.

ACC: Address: E0H **Reset Value: 00h**

7	6	5	4	3	2	1	0
ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0

ACC is the Accumulator register, used for data operations.

P0: Address: 80H **Reset Value: FFh**

7	6	5	4	3	2	1	0
				P0.3	P0.2	P0.1	P0.0

Data setting of Output/Input port P0.

CKCON: Address: 8EH **Reset Value: 00h**

7	6	5	4	3	2	1	0
						TCS1	TCS0

TCS1 = 0: Timer 1 counts once every 12 clocks

TCS1 = 1: Timer 1 counts once every 3 clocks

TCS0 = 0: Timer 0 counts once every 12 clocks

TCS0 = 1: Timer 0 counts once every 3 clocks

PSW (Program Status Word): Address: D0H **Reset Value: 00h**

7	6	5	4	3	2	1	0
CY	AC	F0	RS1	RS0	OV	F1	PARITY

The Program Status Word contains program status information.

Bit Number	Bit Mnemonic	Description
7	CY	Carry Flag, used to indicate the result of arithmetic operation whether a carry or borrow occurred in the 7th bit. Operation result of Addition: CY = 1: a carry occurred; CY = 0: no carry occurred. Operation result of Subtraction: CY = 1: a borrow occurred; CY = 0: no borrow occurred.
6	AC	Auxiliary-Carry Flag, used to indicate the result of arithmetic operation whether the 3rd bit borrow (or carry) from the 4th bit occurred. Operation result of Addition: AC = 1: a carry occurred; AC = 0: no carry occurred. Operation result of Subtraction: AC = 1: a carry occurred; AC = 0: no carry occurred.
5	F0	General purpose flag, can be served as common read/write bit.
4	RS1	Register Bank Select bits 1 and 0 (refer to Register Bank Selection Table).
3	RS0	
2	OV	Overflow Flag, used to indicate the result of arithmetic operation whether an overflow occurred. If OV = 1, an overflow occurred. Otherwise, it is cleared.
1	F1	General-purpose flag, can be served as common read/write bit.
0	P	Parity Flag. It is set to indicate an odd number of “1” bits in the accumulator. Otherwise, it is cleared.

Register Bank Selection Table:

Register Bank	Address	RS1	RS0
0	00H ~ 07H	0	0
1	08H ~ 0FH	0	1
2	10H ~ 17H	1	0
3	18H ~ 1FH	1	1

SP (Stack Point) Address: 81H **Reset Value: 07h**

7	6	5	4	3	2	1	0
SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

Stack Pointer, indicated the location at which the last byte was pushed onto the stack. It is incremented before data is stored during PUSH.

DPL0 (DPTR0, low byte of the 16-bit data pointer 0) Address: 82H **Reset Value: 00h**

7	6	5	4	3	2	1	0
DPL0.7	DPL0.6	DPL0.5	DPL0.4	DPL0.3	DPL0.2	DPL0.1	DPL0.0

DPL0 is a low byte of DPTR0, using together with the data pointer of DPH0.

DPH0 (DPTR0, high byte of the 16-bit data pointer 0) Address: 83H **Reset Value: 00h**

7	6	5	4	3	2	1	0
DPH0.7	DPH0.6	DPH0.5	DPH0.4	DPH0.3	DPH0.2	DPH0.1	DPH0.0

DPH0 is a high byte of DPTR0, using together with the data pointer of DPL0.

Note: Other special function registers will be discussed in later sections.

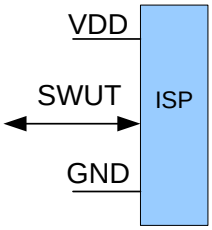
5.5 In-System Programming (ISP) (Important!!! Must Read!!!)

In-System Programming function allows users to perform programming on the target board directly without removing any components.

ISP interface adopts:

3-wire: VDD, GND (VSS), SWUT
2-wire: SWUT, GND (VSS), if the target board already has VDD power.

The figure below illustrates pins of ISP interface:



Note: See WT56F116S/108S WLINK-SWUT ISP User's Manual for more details.

5.5.1 In-System Programming Notice

Condition: MCU SOURCE clock 2~16 MHz (Internal/External Oscillator). For more details, please refer to Chapter 8 Application Circuits.

Description: Because this series of MCU adopts single-wire UART (SWUT) for system programming and the baud rate is 115200 bps, SOURCE clock of MCU must work at 2~16 MHz. In addition, the default setting of MCU is IRC 12 MHz (Source clock /2, MCU works at 6 MHz), and thus direct In-System Programming is supported. It requires adding trigger or wakeup conditions if MCU works at external 1 MHz, Green Mode, Idle Mode or Sleep Mode, otherwise programming procedures will fail. The following section will explain how to operate in those modes. (For more details on ISP reference clock sources, please refer to section 3.1.)

RESET/SWUT pin supports Reset/Programming function at the same time, but each level is different. Please refer to the table below.

Function (V_{DD} = 3.3V)	VIH	VIL
SWUT	0.79 VDD	0.60 VDD
NRST	0.42 VDD	0.20 VDD

Function (V_{DD} = 2.4V)	VIH	VIL
SWUT	0.77 VDD	0.54 VDD
NRST	0.47 VDD	0.22 VDD

Normal Mode:

If MCU works at 2~16 MHz (Internal/External Oscillator) and MCU performs Power On Reset normally, the programming process can go smoothly.

MCU works together with special frequency External Oscillator, such as 1 MHz, 32.768 kHz cryatal oscillator. It requires setting ISP Clock Source Control Register (ISP_CHG_CTL) to enable two control bits (Bit7 ISP_CHG_12M & Bit5 UART_ISP_CHG), which allows SWUT pin to receive trigger signal. After the MCU being switched to Internal Oscillator 12 MHz automatically, the programming process will succeed. For more details, please refer to section 6.7.

Green Mode:

It is so-called Green Mode when MCU works at 32 kHz (Internal/External Oscillator). MCU cannot perform programming directly when works at this mode. It requires setting ISP Clock Source Control Register (ISP_CHG_CTL) to enable two control bits (Bit7 ISP_CHG_12M & Bit5 UART_ISP_CHG), which allows SWUT pin to receive trigger signal. After the MCU being switched to Internal Oscillator 12 MHz automatically, the programming process will succeed. For more details, please refer to section 6.7.

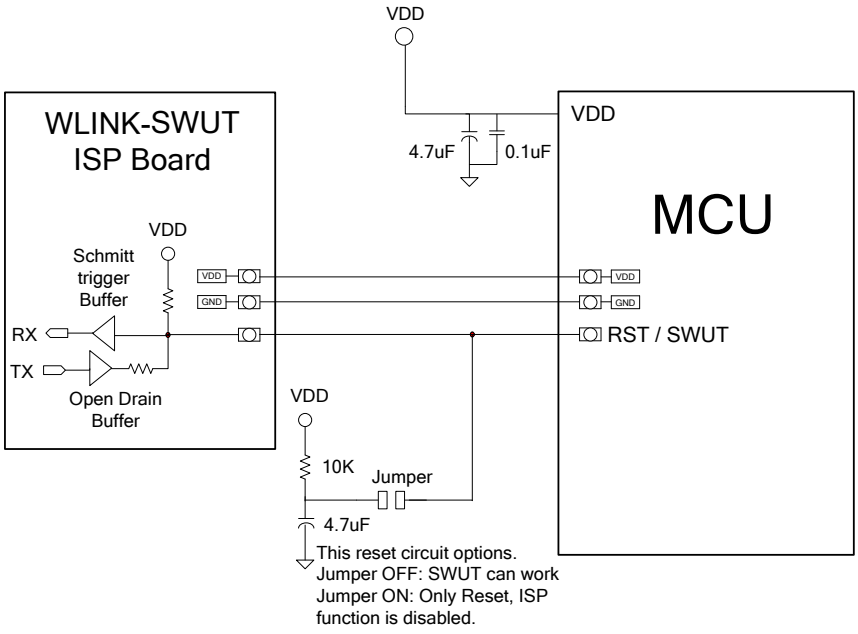
Idle Mode:

Before entering this mode, in addition to setting ISP Clock Source Control Register (ISP_CHG_CTL) to enable two control bits (Bit7 ISP_CHG_12M & Bit5 UART_ISP_CHG), be sure to set up wakeup conditions. Then MCU can switch back to work at 12 MHz, and maintain 2 ~ 3 seconds to receive the programming command from SWUT. For more details, please refer to section 6.7.

Sleep Mode:

Before entering this mode, in addition to setting ISP Clock Source Control Register (ISP_CHG_CTL) to enable two control bits (Bit7 ISP_CHG_12M & Bit5 UART_ISP_CHG), be sure to set up wakeup conditions. Then MCU can switch back to work at 12 MHz, and maintain 2 ~ 3 seconds to receive the programming command from SWUT. For more details, please refer to section 6.7.

Recommended Circuit:



5.6 Timer/Counter

The WT56F116S/108S contains two 16-bit Timer/Counters (Timer0 ~ 1). Both Timer/Counters can be configured as Timer or Counter.

The internal Timer/Counter 0 and Timer/Counter 1 of WT56F116S/108S have four operation modes to be selected by bits M11, M10, or M01, M00 respectively in the Special Function Register TMOD, as described below.

TMOD (8052 Timer0/1 mode control register) Address: 89H

7	6	5	4	3	2	1	0
GATE1	C1/T1	M11	M10	GATE0	C0/T0	M01	M00

Bit Number	Bit Mnemonic	Description
7	GATE1	GATE1 = 1, invalid GATE1 = 0, configured as internal Timer. If TR1 = 1, Timer1 starts.
6	C1/T1	Timer/Counter 1 selector C1/T1 = 1, invalid C1/T1 = 0, configured as an internal Timer, and the counter signal is from MCU Clock 12 MHz IRC ÷ 12
5-4	M11-M10	Timer/Counter 1 mode selection bits 00: Mode 0, 13-bit Timer/Counter 01: Mode 1, 16-bit Timer/Counter 10: Mode 2, 8-bit auto-reload Timer/Counter 11: Mode 3, Timer/Counter 1 stopped and retained count
3	GATE0	GATE0 = 1, invalid GATE0 = 0, configured as internal Timer. If TR0 = 1, Timer0 starts.
2	C0/T0	Timer/Counter 0 selector C0/T0 = 1, invalid C0/T0 = 0, configured as an internal Timer, and the counter signal is from MCU Clock 12 MHz IRC ÷ 12
1-0	M01-M00	Timer/Counter 0 mode selection bits 00: Mode 0, 13-bit Timer/Counter 01: Mode 1, 16-bit Timer/Counter 10: Mode 2, 8-bit auto-reload Timer/Counter 11: Mode 3, 8-bit Timer/Counter (TL0 uses TR0 bit and TH0 uses TR1 bit)

Note: When use Timer/Counter 0 & Timer/Counter1, Cx/Tx must be set as "0" and then Timer/Counter can work normally.

TCON (8052 Timer 0/1 control register) Address: 88H

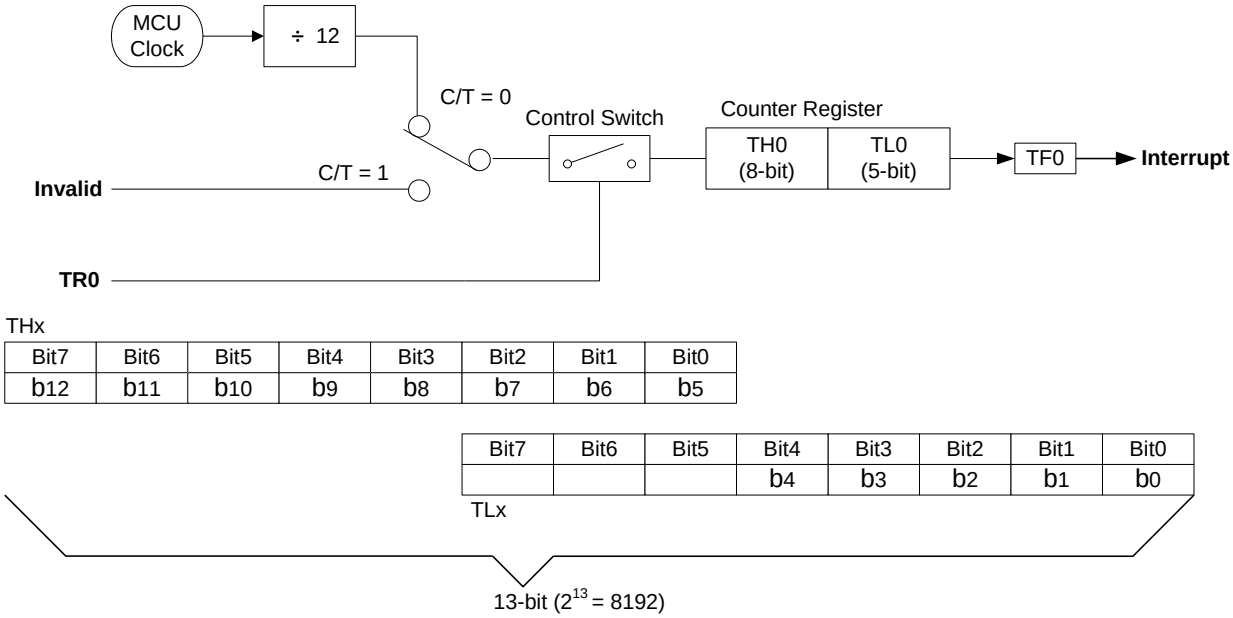
7	6	5	4	3	2	1	0
TF1	TR1	TF0	TR0	-	-	-	-

Bit Number	Bit Mnemonic	Description
7	TF1	Timer/Counter 1 Overflow Flag. When the Timer/Counter overflows, TF1 is set (TF1 = 1). When CPU is jumped to the Interrupt Service Routine of Timer/Counter 1, TF1 is auto-cleared (TF1 = 0).
6	TR1	Timer/Counter 1 Enable bit. If TR1 is set (TR1 = 1), Timer/Counter

Bit Number	Bit Mnemonic	Description
		1 is in use; If TR1 is disabled (TR1 = 0), Timer/Counter 1 stopped.
5	TF0	Timer/Counter 0 Overflow Flag. When the Timer/Counter overflows, TF0 is set (TF0 = 1). When the CPU is jumped to the Interrupt Service Routine of Timer/Counter 0, TF0 is auto-cleared (TF0 = 0).
4	TR0	Timer/Counter 0 Enable bit. If TR0 is set (TR0=1), Timer/Counter 0 is in use; If TR0 is disabled (TR0=0), Timer/Counter 0 stopped.
3-0	-	Invalid

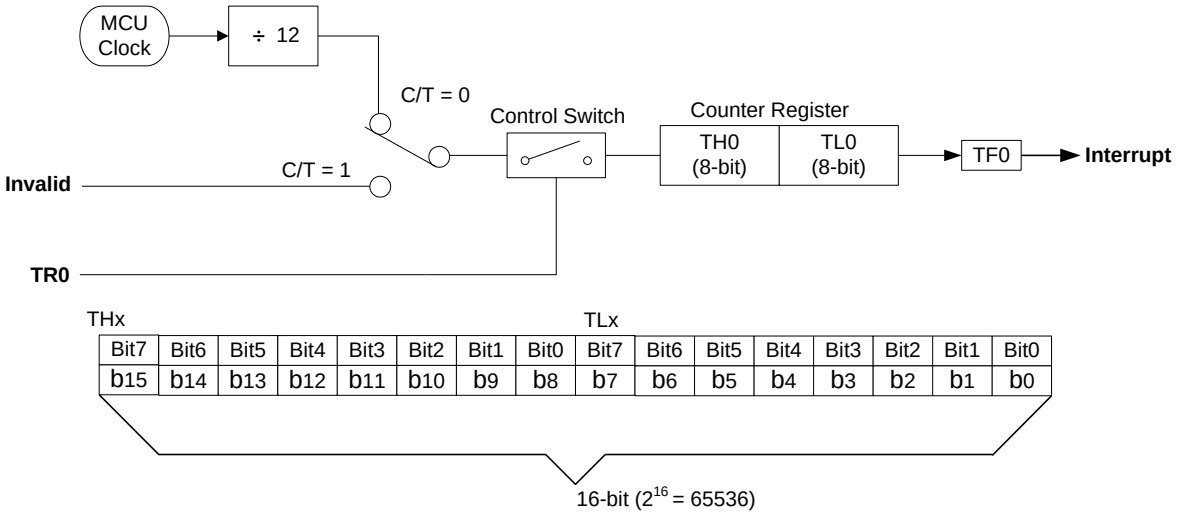
Note: See section 6.4 for more information on Baud rate generator of Timer/Counter 1.

Mode 0:



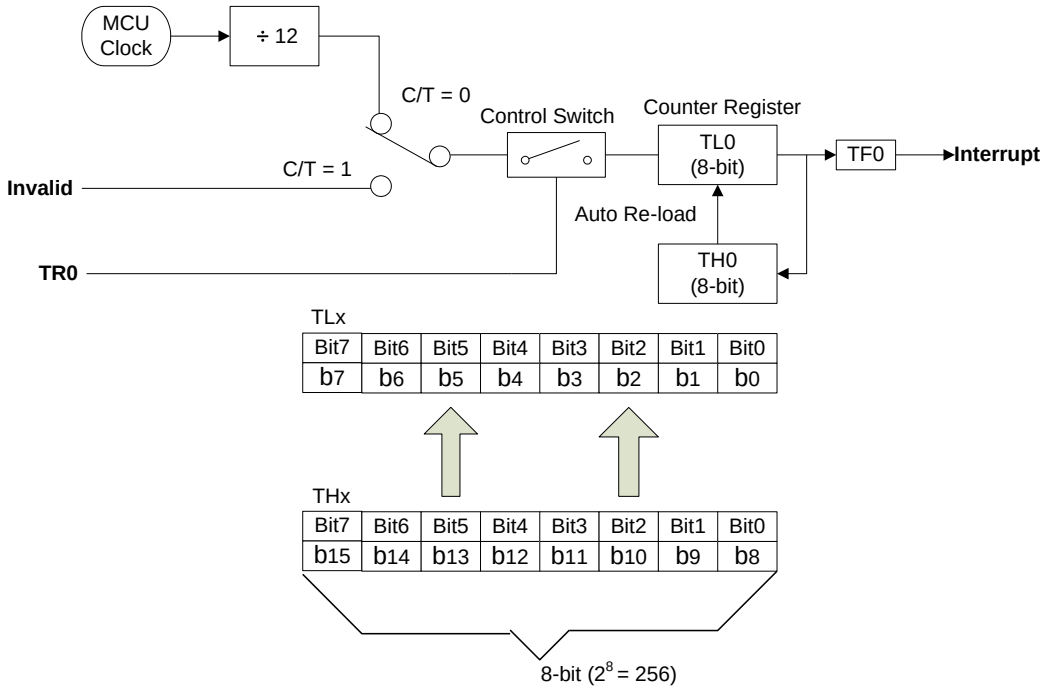
Mode 0 operation is the same for Timer/Counter 0 and Timer/Counter 1. In this mode, the timer register is configured as a 13-bit Up Timer/Counter, which is consists of the Special Function Register THx and TLx. As the count of the 13 bits is all 1s, if the register incremented 1 then count of the 13 bits is all 0s and meantime if the Timer/Counter Interrupt is enabled, an Timer overflow interrupt will occur and Overflow Flag is set (TFx = 1, and TFx locates in TCON of the Special Function Register).

Mode 1:



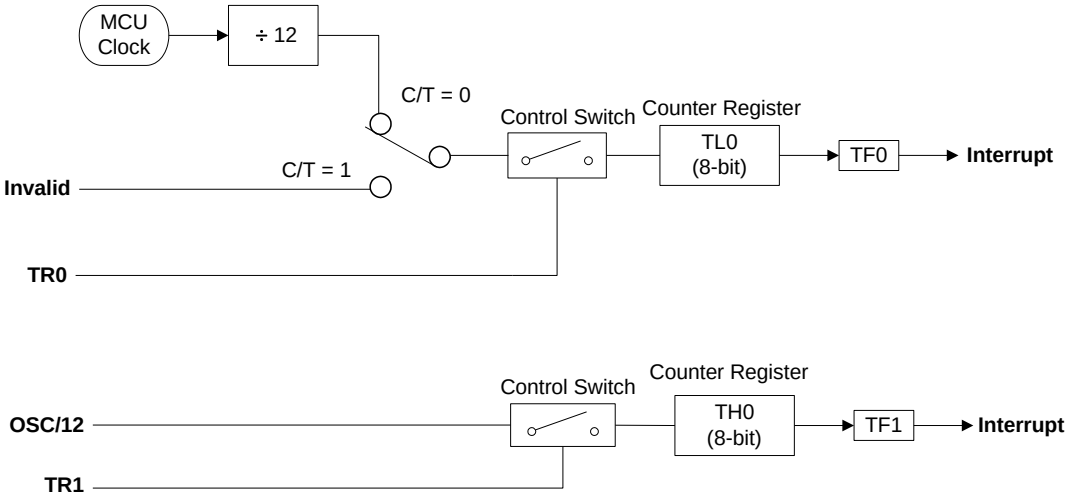
Mode 1 operation is the same as Mode 0 for Timer/Counter 0 and Timer/Counter 1, except that the Timer Register which consists of THx and TLx is configured as a 16-bit Up Timer/Counter.

Mode 2:



Mode 2 operation is the same for Timer/Counter 0 and Timer/Counter 1 to configure two 8-bit auto-reload Timer/Counters. The counter value is stored in TLx Register. Overflow from TLx not only sets TFx = 1, but also auto-reloads contents of THx to TLx.

Mode 3:



Mode 3 operation is rarely different for Timer/Counter 0 and Timer/Counter 1, as described below.
In Mode 3, TL0 is an 8-bit Timer/Counter, while TH0 is an 8-bit Counter controlled by TR1. In the meantime, be aware of the Overflow Flag of Timer/Counter 1 borrowed by TH0, and the corresponding Interrupt Service Routine address is 001BH. In Mode 3, Timer/Counter 1 stopped and retained count.

5.7 Reset

The WT56F116S/108S has seven reset generation sources: Power On Reset (POR), Low Voltage Reset (LVR), Low Voltage Detection Reset (LVDR), External NRST pin Reset Flag, Watchdog Reset, ISP/ICE Command Reset, and PC Counter Overflow Reset (PC_OVR). During Reset, almost all registers are reset to their initial values. You may judge what kind of reset is generated by Reset Flag Register (XFR 0x03).

Power-on Reset (POR)

The Power-on Reset occurs when the VDD supply voltage is below the Power-on Reset voltage threshold (refer to DC Characteristics sections for more details), then XFR: 0x03 POR_RST_FLG = 1.

Low Voltage Reset (LVR)

A reset occurs when the VDD voltage is below the operating voltage threshold, then XFR: 0x03 LVR_RST_FLG = 1.

Low Voltage Detection Reset (LVDR)

A reset occurs when the VDD voltage is below the Low Voltage Detection setting level, then XFR: 0x03 LVD_RST_FLG = 1.

External NRST pin Reset

A reset occurs when the voltage of the external reset pin (NRST) is below its VIL (refer to DC characteristics sections for more details), then XFR: 0x03 NRST_FLG = 1.

Watchdog Timer Reset

A reset occurs when the Watchdog Timer times out, then XFR: 0x03 WDT_RST_FLG = 1.

ISP/ICE Command Reset

An ISP/ICE reset occurs when SWUT pin transmitted the reset command, then XFR: 0x03 ISP_RST_FLG = 1.

PC Counter Overflow Reset (PC_OVR)

The PC counter stores the address where the current instruction locates. A reset occurs when the address exceeds the range of the Flash memory (Flash Address 0x0000 ~ 0x1FFF), then XFR: 0x03 PC_OVL_RST_FLG = 1.

Reset status

When above condition occurred, all Special Function Registers are set to their initial values. SFR contents are described in the following text. XFR contents will be discussed in next section.

The initial value of Special Function Register after Reset (as shown below):

SFR	Initial Value	SFR	Initial Value
P0	11111111b	SCON0	00000000b
SP	00000111b	SBUF0	00000000b
DPL0	00000000b	SBRG0H	00000000b

SFR	Initial Value	SFR	Initial Value
DPH0	00000000b	SBRG0L	00000000b
PCON	00000000b	IE	00000000b
TCON	00000000b	IP	xx000000b
TMOD	00000000b	PSW	00000000b
TL0	00000000b	ACC	00000000b
TL1	00000000b	B	00000000b
TH0	00000000b	XICON	00000000b
TH1	00000000b	CKCON	00000000b

Reset Flag Register RESET_FLG (XFR: 0x03) **Reset Value: 01h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	R	R	R	R	R	R	R
Name	CLR_RST_FLG	PC_OVL_RST_FLG	ISP_RST_FLG	WDT_RST_FLG	NRST_FLG	LVD_RST_FLG	LVR_RST_FLG	POR_RST_FLG

Bit Number	Bit Mnemonic	Description
7	CLR_RST_FLG	1: Clear all Reset Flag
6	PC_OVL_RST_FLG	1: Reset source is from program counter overflow
5	ISP_RST_FLG	1: Reset source is from ISP
4	WDT_RST_FLG	1: Reset source is from Watchdog
3	NRST_FLG	1: Reset source is from External Reset pin
2	LVD_RST_FLG	1: Reset source is from Low Voltage Detection Reset
1	LVR_RST_FLG	1: Reset source is from Low Voltage Reset
0	POR_RST_FLG	1: Reset source is from External Power Reset

5.8 System Clock and Clock sources

The WT56F116S/108S contains two clock sources: DC ~ 24 MHz external crystal oscillator, and internal 12/24 MHz RC oscillator. The MCU clock sources are selected by External Special Function Register (XFR) SOURCE_CLK_SLT[1:0] and MCU_CLK_SLT[1:0]. The initial value is internal 12 MHz RC oscillator and Source Clock/2, at the same time MCU works at 6 MHz operating frequency. For more details, refer to section 6.7 Power Management.

Clock Sources are listed below.

Main Clock Sources	Sub Clock Sources
DC ~ 24 MHz Crystal Oscillator	32K Internal RC Oscillator
12/24 MHz Internal RC Oscillator	32K Internal RC Oscillator
12/24 MHz Internal RC Oscillator	32.768 kHz Crystal Oscillator

6. Enhanced Function

6.1 External Special Function Register (XFR)

External Special Function Register (XFR) locates from 0x00 to 0xFF, must be accessed by the execution of MOVX instruction. It does not support MOVX @R0,A; MOVX A,@R0, and C language does not support the use of data.

`

External Special Function Register table:

External memory address	Description
0000H ~ 000DH	System Register and Reset Register
0010H ~ 001FH	General-purpose I/O port Register
0020H ~ 002FH	General-purpose I/O port Register and Multi-function Register
0030H ~ 003FH	Interrupt Enable Register
0040H ~ 004FH	External Interrupt Request Register (IRQ)
0050H ~ 005FH	Pulse Width Modulation Register (PWM)
0060H ~ 006FH	Wakeup Register
0070H ~ 007FH	Internal Oscillator Calibration Register, Watchdog Register, Watch Timer Register
0080H ~ 00A7H	LCD Driver Display Register
00A8H ~ 00AFH	LCD Driver Register
00B0H ~ 00BFH	Enhanced Timer/Counter Register
00D0H ~ 00D7H	10-bit Analog/Digital Register
00E0H ~ 00EFH	Simulated E²PROM Register

When the Reset status which is mentioned in section 5.7 occurred, the default value of external function register after reset is listed below:

Register Name	Address	Reset Default (Hex)	Index Section
Reserved	-	-	-
System Control Register	0x01	80	6.9
Low Voltage Detection Control Register	0x02	A6	6.17; 6.18
Reset Flag Register	0x03	01	6.18
ISP Clock Source Control Register	0x04	00	6.7
System Clock Source Control Register	0x05	A0	6.7
Power Saving Control Register	0x06	50	6.7
Clock Source Control Register	0x07	A2	6.7
Oscillator Driver Control Register	0x08	58	6.7
External Clock Source Prescaler Control Register 1	0x09	01	6.9
External Clock Source Prescaler Control Register 2	0x0A	76	6.9
Low Voltage Reset Control Register	0x0C	00	6.16
Customer Code Register 1	0x0D	FF	6.20
Customer Code Register 2	0x0E	FF	6.20
Customer Code Register 3	0x0F	FF	6.20
General-purpose I/O Port A Output Enable Control Register	0x10	00	6.2

Register Name	Address	Reset Default (Hex)	Index Section
General-purpose I/O Port B Output Enable Control Register	0x11	00	6.2
General-purpose I/O Port C Output Enable Control Register	0x12	00	6.2
General-purpose I/O Port D Output Enable Control Register	0x13	00	6.2
General-purpose I/O Port E Output Enable Control Register	0x14	00	6.2
General-purpose I/O port F Output Enable Control Register	0x15	00	6.2
General-purpose I/O port G Output Enable Control Register	0x16	00	6.2
General-purpose I/O Port A Data Register	0x17	00	6.2
General-purpose I/O Port B Data Register	0x18	00	6.2
General-purpose I/O Port C Data Register	0x19	00	6.2
General-purpose I/O Port D Data Register	0x1A	00	6.2
General-purpose I/O Port E Data Register	0x1B	00	6.2
General-purpose I/O Port F Data Register	0x1C	00	6.2
General-purpose I/O Port G Data Register	0x1D	00	6.2
General-purpose I/O Port A Enable Internal Pull-up Resistor Register	0x1E	FF	6.2
General-purpose I/O Port B Enable Internal Pull-up Resistor Register	0x1F	FF	6.2
General-purpose I/O Port C, D, E, F, G Enable Internal Pull-up Resistor Register	0x20	F8	6.2
General-purpose I/O Port A Output Type Control Register	0x22	FF	6.2
General-purpose I/O Port B Output Type Control Register	0x23	FF	6.2
General-purpose I/O Port A Complex Function Setting Register 1	0x25	00	6.2
General-purpose I/O Port A Complex Function Setting Register 2	0x26	00	6.2
General-purpose I/O Port B Complex Function Setting Register 1	0x27	00	6.2
General-purpose I/O Port B Complex Function Setting Register 2	0x28	00	6.2
General-purpose I/O Port C Complex Function Setting Register	0x29	00	6.2
General-purpose I/O Port D Complex Function Setting Register	0x2A	00	6.2
General-purpose I/O Port E Complex Function Setting Register	0x2B	00	6.2
General-purpose I/O Port F Complex Function Setting Register 1	0x2C	00	6.2
General-purpose I/O Port F Complex Function Setting Register 2	0x2D	00	6.2
General-purpose I/O Port G Complex Function Setting Register	0x2E	00	6.2
General-purpose I/O Port Extend Complex Function Setting Register	0x2F	00	6.2
8052 External Interrupt 0 Control Register	0x30	00	6.3
8052 External Interrupt 1 Control Register	0x31	00	6.3
8052 External Interrupt 3 Control Register	0x34	00	6.3
8052 External Interrupt 0 (INT0) Flag Register	0x35	00	6.3
8052 External Interrupt 1 (INT1) Flag Register	0x36	00	6.3
8052 External Interrupt 3 (INT3) Flag Register	0x39	00	6.3

Register Name	Address	Reset Default (Hex)	Index Section
External Interrupt Request (IRQ) Control Register	0x40	00	6.5
External Interrupt Request (IRQ) Status Register	0x41	00	6.5
External Interrupt Request (IRQ) Clear Register	0x42	00	6.5
External Interrupt Request (IRQ) Bi-directional Trigger Register	0x43	00	6.5
External Interrupt Request (IRQ) Trigger Edge Register	0x44	00	6.5
PWM Control Register	0x50	00	6.6
PWM0 Period Control High Bytes Register	0x51	00	6.6
PWM0 Period Control Low Bytes Register	0x52	01	6.6
PWM0 Duty Cycle Control High Bytes Register	0x53	00	6.6
PWM0 Duty Cycle Control Low Bytes Register	0x54	00	6.6
PWM1 Period Control High Bytes Register	0x55	00	6.6
PWM1 Period Control Low Bytes Register	0x56	01	6.6
PWM1 Duty Cycle Control High Bytes Register	0x57	00	6.6
PWM1 Duty Cycle Control Low Bytes Register	0x58	00	6.6
General-purpose I/O Port Wakeup Control Register 1	0x60	00	6.7
General-purpose I/O Port Wakeup Control Register 2	0x61	00	6.7
Peripheral Interrupt Wakeup Control Register	0x64	00	6.7
General-purpose I/O Port Wakeup Flag Register 1	0x65	00	6.7
General-purpose I/O Port Wakeup Flag Register 2	0x66	00	6.7
Peripheral Interrupt Wakeup Flag Register	0x69	00	6.7
Wakeup Clear Register	0x6A	00	6.7
Internal Oscillator Adjust Register	0x70	40	6.8
Internal Oscillator Counter Data High Bytes Register	0x71	00	6.8
Internal Oscillator Counter Data Low Bytes Register	0x72	00	6.8
Internal Oscillator Calibration Control Register	0x73	00	6.8
Watchdog Timer Control Register	0x78	02	6.9
Watch Timer Control Register	0x7C	80	6.9
Watch Timer Output Selection Register	0x7D	00	6.9
LCD Driver Display Data Register 0	0x80	00	6.10
LCD Driver Display Data Register 1	0x81	00	6.10
LCD Driver Display Data Register 2	0x82	00	6.10
LCD Driver Display Data Register 3	0x83	00	6.10
LCD Driver Display Data Register 4	0x84	00	6.10
LCD Driver Display Data Register 5	0x85	00	6.10
LCD Driver Display Data Register 6	0x86	00	6.10
LCD Driver Display Data Register 7	0x87	00	6.10
LCD Driver Display Data Register 8	0x88	00	6.10

Register Name	Address	Reset Default (Hex)	Index Section
LCD Driver Display Data Register 9	0x89	00	6.10
LCD Driver Display Data Register 10	0x8A	00	6.10
LCD Driver Display Data Register 11	0x8B	00	6.10
LCD Driver Display Data Register 12	0x8C	00	6.10
LCD Driver Display Data Register 13	0x8D	00	6.10
LCD Driver Display Data Register 14	0x8E	00	6.10
LCD Driver Display Data Register 15	0x8F	00	6.10
LCD Driver Display Data Register 16	0x90	00	6.10
LCD Driver Display Data Register 17	0x91	00	6.10
LCD Driver Display Data Register 18	0x92	00	6.10
LCD Driver Display Data Register 19	0x93	00	6.10
LCD Driver Display Data Register 20	0x94	00	6.10
LCD Driver Display Data Register 21	0x95	00	6.10
LCD Driver Display Data Register 22	0x96	00	6.10
LCD Driver Display Data Register 23	0x97	00	6.10
LCD Driver Display Data Register 24	0x98	00	6.10
LCD Driver Display Data Register 25	0x99	00	6.10
LCD Driver Display Data Register 26	0x9A	00	6.10
LCD Driver Display Data Register 27	0x9B	00	6.10
LCD Driver Display Data Register 28	0x9C	00	6.10
LCD Driver Display Data Register 29	0x9D	00	6.10
LCD Driver Display Data Register 30	0x9E	00	6.10
LCD Driver Display Data Register 31	0x9F	00	6.10
LCD Driver Control Register 1	0xA8	00	6.10
LCD Driver Control Register 2	0xA9	00	6.10
LCD Driver Segment Output Enable Register 1	0xAB	00	6.10
LCD Driver Segment Output Enable Register 2	0xAC	00	6.10
LCD Driver Segment Output Enable Register 3	0xAD	00	6.10
LCD Driver Segment Output Enable Register 4	0xAE	00	6.10
Enhanced Timer/Counter Control Register	0xB0	00	6.12
Enhanced Timer/Counter Interrupt Register	0xB2	00	6.12
Enhanced Timer/Counter Data Buffer Low Bytes Register	0xB3	00	6.12
Enhanced Timer/Counter Data Buffer High Bytes Register	0xB4	80	6.12
Master/Slave I^2C Control Register 0	0xB8	40	6.11
Master/Slave I^2C Status Register 0	0xB9	00	6.11
Master/Slave I^2C Transmit Buffer Register 0	0xBA	00	6.11
Master/Slave I^2C Transmit and Receive Buffer Register 0	0xBB	FF	6.11

Register Name	Address	Reset Default (Hex)	Index Section
Slave I²C Address Register 0	0xBC	00	6.11
Master/Slave I²C Extend Control Register 0	0xBD	00	6.11
SPI Control Register 1	0xC0	00	6.15
SPI Control Register 2	0xC1	00	6.15
SPI Interrupt Control Register	0xC2	00	6.15
SPI Interrupt Clear Register	0xC3	00	6.15
SPI Flag Register	0xC4	00	6.15
SPI Bit Rate Setting Register	0xC5	00	6.15
SPI Transmit Buffer Register	0xC6	FF	6.15
SPI Receive Buffer Register	0xC7	00	6.15
Master/Slave I²C Control Register 1	0xC8	40	6.11
Master/Slave I²C Status Register 1	0xC9	00	6.11
Master/Slave I²C Transmit Buffer Register 1	0xCA	00	6.11
Master/Slave I²C Transmit and Receive Buffer Register 1	0xCB	FF	6.11
Slave I²C Address Register 1	0xCC	00	6.11
Master/Slave I²C Extend Control Register 1	0xCD	00	6.11
ADC Control Register	0xD0	80	6.13
ADC Setting Control Register	0xD1	40	6.13
ADC Interrupt Control Register	0xD2	00	6.13
ADC Channel Control Register	0xD3	00	6.13
ADC Voltage Compare Data High Bytes Register	0xD4	80	6.13
ADC Voltage Compare Data Low Bytes Register	0xD5	00	6.13
ADC Converted Data High Bytes Register	0xD6	00	6.13
ADC Converted Data Low Bytes Register	0xD7	00	6.13
DAC Converted Control Register	0xD8	80	6.14
DAC Converted Data High Bytes Register	0xD9	00	6.14
DAC Converted Data Low Bytes Register	0xDA	00	6.14
E²PROM Enable Register 1	0xE0	00	6.19
E²PROM Enable Register 2	0xE1	00	6.19
E²PROM Address Low Bytes Register	0xE2	FF	6.19
E²PROM Address High Bytes Register	0xE3	07	6.19
E²PROM Control Register	0xE4	00	6.19
E²PROM Break Register	0xE6	00	6.19
E²PROM Data Register	0XE8	00	6.19

6.2 I/O Port

6.2.1 Features

- 45 programmable I/O, contains: GPIOA[7:0], GPIOB[7:0], GPIOC[7:3], GPIOD[7:0], GPIOE[7:0], GPIOF[7:0], and GPIOG[7:6] (PB6 and PF4 are not included)
- Some I/O with special functions (such as LCD, ADC, and PWM etc.), can be configured by Special Function Register

6.2.2 Register

WT56F116S/108S I/O related registers are classified into four categories:

- GPIOx_OE: Control Output/Input Register, configured to set I/O as output or input. If the corresponding bit GPIOx_OE = 1, it is an output port with 4 mA driving ability
- GPIOx_D: Data Register, reading I/O data or set output of I/O
- GPIOx_PHN: Internal Pull-up resistor Enable Register. When I/O is configured as Input port (by GPIOx_OE), this register is allowed to set if I/O is with pull-up resistor. If the corresponding GPIOx_PHN bit = 0, the I/O is with internal pull-up resistor. The internal pull-up Resistor Enable Register of the General-purpose I/O port C~G is the same register, each bit defines one I/O port
- GPIOx_TYP: Output mode setting Register, is configured to set I/O as Push-Pull or Open-Drain type. Only GPIOA[7:0], or GPIOB[7:0] is allowed to set output type while others are push-pull type

General-purpose I/O Port A Output Enable Control Register GPIOA_OE (XFR: 0x10) **Reset Value: 00h**
General-purpose I/O Port B Output Enable Control Register GPIOB_OE (XFR: 0x11) **Reset Value: 00h**
General-purpose I/O Port D Output Enable Control Register GPIOD_OE (XFR: 0x13) **Reset Value: 00h**
General-purpose I/O Port E Output Enable Control Register GPIOE_OE (XFR: 0x14) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOx_OE[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOA_OE[7:0] GPIOB_OE[7:0] GPIOD_OE[7:0] GPIOE_OE[7:0]	General-purpose I/O Port A, B, D, E Output/Input setting 1: output 0: input (default)

General-purpose I/O Port C Output Enable Control Register GPIOC_OE (XFR: 0x12) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	-	-	-
Name	GPIOC_OE[7:3]					Reserved		

Bit Number	Bit Mnemonic	Description
7-3	GPIOC_OE[7:3]	General-purpose I/O Port C Output/Input setting 1: output 0: input (default)
2-0	Reserved	-

General-purpose I/O Port F Output Enable Control Register GPIOF_OE (XFR: 0x15) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W
Name	GPIOF_OE[7:5]			Reserved	GPIOF_OE[3:0]			

Bit Number	Bit Mnemonic	Description
7-0	GPIOF_OE[7:0]	General-purpose I/O Port F Output/Input setting 1: output 0: input (default)
4	Reserved	-
3-0	GPIOF_OE[3:0]	General-purpose I/O Port F Output/Input setting 1: output 0: input (default)

- **: unimplemented.**

General-purpose I/O port G Output Enable Control Register GPIOG_OE (XFR: 0x16) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	-	-	-	-	-	-
Name	GPIOG_OE[7:6]		Reserved					

Bit Number	Bit Mnemonic	Description
7-6	GPIOG_OE[7:6]	General-purpose I/O Port G Output/Input setting 1: output 0: input (default)
5-0	Reserved	-

General-purpose I/O Port A Data Register GPIOA_D (XFR: 0x17) **Reset Value: 00h**
General-purpose I/O Port B Data Register GPIOB_D (XFR: 0x18) **Reset Value: 00h**
General-purpose I/O Port D Data Register GPIOD_D (XFR: 0x1A) **Reset Value: 00h**
General-purpose I/O Port E Data Register GPIOE_D (XFR: 0x1B) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOx_D[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOA_D[7:0] GPIOB_D[7:0] GPIOD_D[7:0] GPIOE_D[7:0]	General-purpose I/O Port A, B, D, E Output/Input data

General-purpose I/O Port C Data Register GPIOC_D (XFR: 0x19) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	-	-	-
Name	GPIOC_D[7:3]					Reserved		

Bit Number	Bit Mnemonic	Description
7-3	GPIOC_D[7:3]	General-purpose I/O Port C Output/Input data
2-0	Reserved	-

General-purpose I/O Port F Data Register GPIOF_D (XFR: 0x1C) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W
Name	GPIOF_D[7:5]			Reserved	GPIOF_D[3:0]			

Bit Number	Bit Mnemonic	Description
7-5	GPIOF_D[7:5]	General-purpose I/O Port F Output/Input data
4	Reserved	-
3-0	GPIOF_D[3:0]	General-purpose I/O Port F Output/Input data

General-purpose I/O Port G Data Register GPIOG_D (XFR: 0x1D) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	-	-	-	-	-	-
Name	GPIOG_D[7:6]		Reserved					

Bit Number	Bit Mnemonic	Description
7-5	GPIOG_D[7:6]	General-purpose I/O Port G Output/Input data
5-0	Reserved	-

General-purpose I/O Port A Enable Internal Pull-up Resistor Register GPIOA_PHN (XFR: 0x1E) **Reset Value: FFh**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOA_PHN[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOA_PHN[7:0]	Enable General-purpose I/O Port A Pull-up Resistor setting 1: Disable Pull-up Resistor (default) 0: Enable Pull-up Resistor

General-purpose I/O Port B Enable Internal Pull-up Resistor Register GPIOB_PHN (XFR: 0x1F) **Reset Value: FFh**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOB_PHN[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOB_PHN[7:0]	Enable General-purpose I/O Port B Pull-up Resistor setting 1: Disable Pull-up Resistor (default) 0: Enable Pull-up Resistor

General-purpose I/O Port C, D, E, F, G Enable Internal Pull-up Resistor Register GPIOCDEFG_PHN (XFR: 0x20)

Reset Value: F8h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	-	-	-
Name	GPIOC_PHN	GPIOD_PHN	GPIOE_PHN	GPIOF_PHN	GPIOG_PHN	Reserved		

Bit Number	Bit Mnemonic	Description
7	GPIOC_PHN	Enable General-purpose I/O Port C Pull-up Resistor setting 1: Disable Pull-up Resistor (default) 0: Enable Pull-up Resistor
6	GPIOD_PHN	Enable General-purpose I/O Port D Pull-up Resistor setting 1: Disable Pull-up Resistor (default) 0: Enable Pull-up Resistor
5	GPIOE_PHN	Enable General-purpose I/O Port E Pull-up Resistor setting 1: Disable Pull-up Resistor (default) 0: Enable Pull-up Resistor
4	GPIOF_PHN	Enable General-purpose I/O Port F Pull-up Resistor setting 1: Disable Pull-up Resistor (default) 0: Enable Pull-up Resistor
3	GPIOG_PHN	Enable General-purpose I/O Port G Pull-up Resistor setting 1: Disable Pull-up Resistor (default) 0: Enable Pull-up Resistor
2-0	Reserved	-

- **: unimplemented.**

General-purpose I/O Port A Output Type Control Register GPIOA_TYP (XFR: 0x22) **Reset Value: FFh**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOA_TYP[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOA_TYP[7:0]	General-purpose I/O Port A output type setting 1: push-pull output type (default) 0: open-drain output type

General-purpose I/O Port B Output Type Control Register GPIOB_TYP (XFR: 0x23) **Reset Value: FFh**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIOB_TYP[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIOB_TYP[7:0]	General-purpose I/O Port B output type setting 1: push-pull output type (default) 0: open-drain output type

6.2.3 Port Sharing

This is used to set I/O functions, such as PWM, ADC, etc.

General-purpose I/O Port A Complex Function Setting Register1 GPIOA_FUN1 (XFR: 0x25) Reset Value: 00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	-	-	-	R/W	-	-
Name	GPA7_FUN_SLT[1:0]		Reserved			GPA5_FUN_SLT	Reserved	

Bit Number	Bit Mnemonic	Description
7-6	GPA7_FUN_SLT[1:0]	Set GPIOA7D complex function 00: GPIO/ETMIA/IRQ0 (default) 01: RXA, RX of path A of UART (select RXA, and will auto define GPIOA6DH as TXA) 10: DAC analog output 11: P00 output/input (mapping to 8052 P0.0)
5-3	Reserved	-
2	GPA5_FUN_SLT	Set GPIOA5D complex function 1: MOSCI1 (served as the Crystal oscillator input pin of path 1, will auto define GPIOA4DH as the crystal oscillator output pin (MOSCO1) instead of GPIO function) 0: GPIO (default), and meanwhile GPIOA4DH will be set as GPIO function. Default value can be selected by section 6.20 Code Option
1-0	Reserved	-

-: unimplemented.

Note 1: The setting of using External Crystal Oscillator as SOURCE clock (using Crystal Oscillator as the input pins of path 1):

1. **Select Crystal Oscillator as the input pins of path 1: MOSCI1, MOSCO1. (XFR 0x08 SLT_CRYSTAL = 0)**
2. **Set GPIOA5 and GPIOA4 as Input port. (XFR 0x10 GPIOA_OE[5:4])**
3. **GPIOA5 and GPIOA4 disable internal pull high resistor. If enable pull high resistor will result in oscillator outputs unstable frequency. (XFR 0x1E GPIOA_PHN[5:4])**
4. **Set GPIOA5 and GPIOA4 as Crystal Oscillator pin. (XFR 0x25 GPA5_FUN_SLT)**
5. **Set the driving ability of External Main Crystal Oscillator. (XFR 0x08 CRY_12M_DR[2:0])**
6. **Power on External Crystal Oscillator switch. (XFR 0x07 CRY_12M_PD)**
7. **Switch SOURCE clock to External Crystal Oscillator sources. (XFR 0x05 SOURCE_CLK_SLT[1:0])**

Note 2: While using UART or 8052 port, please set the mapping output type of GPIOA_TYP as open-drain and connect to pull-high resistor.

General-purpose I/O Port A Complex Function Setting Register2 GPIOA_FUN2 (XFR: 0x26) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved	GPA3_FUN_SLT	GPA2_FUN_SLT[1:0]		GPA1_FUN_SLT[1:0]		GPA0_FUN_SLT[1:0]	

Bit Number	Bit Mnemonic	Description
7	Reserved	-
6	GPA3_FUN_SLT	Set GPIOA3DH complex function 1: PWM0B, PWM0 output of path B 0: GPIO/ETMIB/IRQ1 (default)
5-4	GPA2_FUN_SLT[1:0]	Set GPIOA2DH complex function 00: GPIO/IRQ2 (default) 01: VREF, ADC reference voltage input 10: PWM0A, PWM0 output of path A 11: P01 output/input (mapping to 8052 P0.1)
3-2	GPA1_FUN_SLT[1:0]	Set GPIOA1DH complex function 00: GPIO/IRQ3/ETMIC (default) 01: ADC11, ADC analog input 10: PWM1A, PWM1 output of path A 11: P02 output/input (mapping to 8052 P0.2)
1-0	GPA0_FUN_SLT[1:0]	Set GPIOA0DH complex function {bit 2 mapping to Register 0x2F bit 0 (GPA0_FUN_SLT2)} 000: GPIO/IRQ4 (default) 001: ADC10, ADC analog input 010: ETMO, Enhanced Timer comparing result output 011: P03 output/input (mapping to 8052 P0.3) 1xx: RX1A/TX1A, PA0 & PA1 are both used for UART1 path A

-: unimplemented.

Note: While using 8052 port, please set the mapping output type of GPIOA_TYP as open-drain and connect to pull-high resistor.

General-purpose I/O Port B Complex Function Setting Register 1 GPIOB_FUN1 (XFR: 0x27) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	-	-	R/W	R/W	R/W	R/W
Name	GPB7_FUN_SLT[1:0]		Reserved	Reserved	GPB5_FUN_SLT[1:0]		GPB4_FUN_SLT[1:0]	

Bit Number	Bit Mnemonic	Description
7-6	GPB7_FUN_SLT[1:0]	Set GPIOB7DH complex function 00: GPIO/IRQ5 (default)) 01: ADC9, ADC analog input 10: PWM1B, PWM1 output of path B 11: reserved
5-4	Reserved	-
3-2	GPB5_FUN_SLT[1:0]	Set GPIOB5DH complex function 00: GPIO/IRQ6 (default) 01: SEG31/ADC7, ADC analog input

Bit Number	Bit Mnemonic	Description
		10: reserved 11: SCL1B
1-0	GPB4_FUN_SLT[1:0]	Set GPIOB4DH complex function 00: GPIO/IRQ7 (default) 01: SEG30/ADC6, ADC analog input 10: PWM0C, PWM0 output of path C 11: SDA1B

-: unimplemented.

General-purpose I/O Port B Complex Function Setting Register2 GPIOB_FUN2 (XFR: 0x28) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPB3_FUN_SLT[1:0]		GPB2_FUN_SLT[1:0]		GPB1_FUN_SLT[1:0]		GPB0_FUN_SLT[1:0]	

Bit Number	Bit Mnemonic	Description
7-6	GPB3_FUN_SLT[1:0]	Set GPIOB3DH complex function 00: GPIO (default) 01: SEG39, LCD SEG output 10: RXB, RX of path B of UART (select RXB, and the mapping GPIOB2DH must be set as GPIO function) 11: SCL0A
5-4	GPB2_FUN_SLT[1:0]	Set GPIOB2DH complex function 00: GPIO (default) 01: SEG28, LCD SEG output 10: reserved 11: SCL0A **Note: If GPIOB3 = RXB, and the mapping GPIOB2DH must be set as GPIO function.**
3-2	GPB1_FUN_SLT[1:0]	Set GPIOB1DH complex function 00: GPIO (default) 01: SEG27/ADC4, LCD SEG output / ADC analog input 10: reserved 11: SDA0A
1-0	GPB0_FUN_SLT[1:0]	Set GPIOB0DH complex function 00: GPIO (default) 01: SEG26/ADC3, LCD SEG output / ADC analog input 10: reserved 11: SDA0B

-: unimplemented.

Note: While using UART, please set the mapping output type of GPIOB_TYP as open-drain and connect to pull-high resistor.

General-purpose I/O Port C Complex Function Setting Register GPIOC_FUN (XFR: 0x29) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	-	-	-
Name	GPC_FUN_SLT[7:3]					Reserved		

Bit Number	Bit Mnemonic	Description
7	GPC7_FUN_SLT	Set GPIOC7 complex function 1: SEG25/ADC2, LCD SEG output / ADC analog input 0: GPIO (default)
6	GPC6_FUN_SLT	Set GPIOC6 complex function 1: SEG24/ADC1, LCD SEG output / ADC analog input 0: GPIO (default)
5	GPC5_FUN_SLT	Set GPIOC5 complex function 1: SEG23/ADC0, LCD SEG output / ADC analog input 0: GPIO (default)
4	GPC4_FUN_SLT	Set GPIOC4 complex function 1: SEG22/ADC15, LCD SEG output 0: GPIO (default)
3	GPC3_FUN_SLT	Set GPIOC3 complex function 1: SEG21, LCD SEG output 0: GPIO (default)
2-0	Reserved	-

General-purpose I/O Port D Complex Function Setting Register GPIOD_FUN (XFR: 0x2A) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPD_FUN_SLT[7:0]							

Bit Number	Bit Mnemonic	Description
7	GPD7_FUN_SLT	Set GPIOD7 complex function 1: SEG20, LCD SEG output 0: GPIO (default)
6	GPD6_FUN_SLT	Set GPIOD6 complex function 1: SEG19, LCD SEG output 0: GPIO (default)
5	GPD5_FUN_SLT	Set GPIOD5 complex function 1: SEG18, LCD SEG output 0: GPIO (default)
4	GPD4_FUN_SLT	Set GPIOD4 complex function 1: SEG17, LCD SEG output 0: GPIO (default)
3	GPD3_FUN_SLT	Set GPIOD3 complex function 1: SEG16, LCD SEG output 0: GPIO (default)
2	GPD2_FUN_SLT	Set GPIOD2 complex function 1: SEG15, LCD SEG output 0: GPIO (default)
1	GPD1_FUN_SLT	Set GPIOD1 complex function 1: SEG14, LCD SEG output 0: GPIO (default)
0	GPD0_FUN_SLT	Set GPIOD0 complex function 1: SEG13/ADC14, LCD SEG output 0: GPIO (default)

General-purpose I/O E Complex Function Setting Register GPIOE_FUN (XFR: 0x2B) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPE_FUN_SLT[7:0]							

Bit Number	Bit Mnemonic	Description
7	GPE7_FUN_SLT	Set GPIOE7 complex function {bit 1 mapping to Register 0x2F bit 7 (GPE7_FUN_SLT2)} 00: GPIO (default) 01: SEG12/ADC13, LCD SEG output 10: SCK 11: TX1B/RX1B
6	GPE6_FUN_SLT	Set GPIOE6 complex function {bit 1 mapping to Register 0x2F bit 6 (GPE6_FUN_SLT2)} 00: GPIO (default) 01: SEG11/ADC12, LCD SEG output 10: MISO 11: reserved
5	GPE5_FUN_SLT	Set GPIOE5 complex function {bit 1 mapping to Register 0x2F bit 5 (GPE5_FUN_SLT2)} 00: GPIO (default) 01: SEG10, LCD SEG output 10: MOSI 11: reserved
4	GPE4_FUN_SLT	Set GPIOE4 complex function {bit 1 mapping to Register 0x2F bit 4 (GPE4_FUN_SLT2)} 00: GPIO (default) 01: SEG9, LCD SEG output 10: STB 11: reserved
3	GPE3_FUN_SLT	Set GPIOE3 complex function 1: SEG8, LCD SEG output 0: GPIO (default)
2	GPE2_FUN_SLT	Set GPIOE2 complex function 1: SEG7, LCD SEG output 0: GPIO (default)
1	GPE1_FUN_SLT	Set GPIOE1 complex function 1: SEG6, LCD SEG output 0: GPIO (default)
0	GPE0_FUN_SLT	Set GPIOE0 complex function 1: SEG5, LCD SEG output 0: GPIO (default)

General-purpose I/O Port F Complex Function Setting Register1 GPIOF_FUN1 (XFR: 0x2C) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	R/W	-	R/W	-	R/W	-	-
Name	Reserved	GPF7_FUN_SLT	Reserved	GPF6_FUN_SLT	Reserved	GPF5_FUN_SLT	Reserved	

Bit Number	Bit Mnemonic	Description
7	Reserved	-
6	GPF7_FUN_SLT	Set GPIOF7 complex function 1: SEG4, LCD SEG output 0: GPIO (default)
5	Reserved	-
4	GPF6_FUN_SLT	Set GPIOF6 complex function 1: SEG3, LCD SEG output 0: GPIO (default)
3	Reserved	-
2	GPF5_FUN_SLT	Set GPIOF5 complex function 1: SEG2, LCD SEG output 0: GPIO (default)
1-0	Reserved	-

-: unimplemented.

General-purpose I/O Port F Complex Function Setting Register2 GPIOF_FUN1 (XFR: 0x2D) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPF3_FUN_SLT[1:0]		GPF2_FUN_SLT[1:0]		GPF1_FUN_SLT[1:0]		GPF0_FUN_SLT[1:0]	

Bit Number	Bit Mnemonic	Description
7-6	GPF3_FUN_SLT[1:0]	Set GPIOF3 complex function 00: GPIO (default) 01: COM3, LCD Common 3 10: SCL1A 11: P07
5-4	GPF2_FUN_SLT[1:0]	Set GPIOF2 complex function 00: GPIO (default) 01: COM2, LCD Common 2 10: SDA1A 11: P06
3-2	GPF1_FUN_SLT[1:0]	Set GPIOF1 complex function 00: GPIO (default) 01: COM1, LCD Common 1 10: MOSCO2, served as the Crystal oscillator output pin of path 2, will auto define GPIOF0 as the crystal oscillator input pins (MOSCI2) instead of GPIO function 11: P05 Default value can be selected by section 6.20 Code Option
1-0	GPF0_FUN_SLT[1:0]	Set GPIOF0 complex function 00: GPIO (default) 01: COM0, LCD Common 0 10: reserved 11: P04

-: unimplemented.

Notes: The setting of using External Crystal Oscillator as SOURCE clock (using Crystal Oscillator as the input pins of path 2):

1. **Select Crystal Oscillator as the input pins of path 2: MOSCI2, MOSCO2. (XFR 0x08 SLT_CRYSTAL = 1)**
2. **Set GPIOF1 and GPIOF0 as Input port. (XFR 0x15 GPIOF_OE[1:0])**
3. **GPIOF1 and GPIOF0 disable internal pull high resistor. If enable pull high resistor will result in oscillator outputs unstable frequency. (XFR 0x20 GPIOF_PHN)**
4. **Set GPIOF1 and GPIOF0 as Crystal Oscillator pin. (XFR 0x2D GPF1_FUN_SLT[1:0])**
5. **Set the driving ability of External Main Crystal Oscillator. (XFR 0x08 CRY_12M_DR[2:0])**
6. **Power on External Crystal Oscillator switch. (XFR 0x07 CRY_12M_PD)**
7. **Switch SOURCE clock to External Crystal Oscillator. (XFR 0x05 SOURCE_CLK_SLT[1:0])**

General-purpose I/O Port G Complex Function Setting Register GPIOG_FUN (XFR: 0x2E) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	-	-	-	-	-	-
Name	GPG_FUN_SLT[7:6]		Reserved					

Bit Number	Bit Mnemonic	Description
7	GPG7_FUN_SLT[7]	Set GPIOG7 complex function 1: SEG1, LCD SEG output 0: GPIO (default)
6	GPG6_FUN_SLT[6]	Set GPIOG6 complex function 1: SEG0, LCD SEG output 0: GPIO (default)
5-0	Reserved	-

General-purpose I/O Extend Complex Function Setting Register GPIOX_FUN (XFR: 0x2F) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	-	-	-	R/W
Name	GPE7_FUN_SLT2	GPE6_FUN_SLT2	GPE5_FUN_SLT2	GPE4_FUN_SLT2	Reserved			GPA0_FUN_SLT2

Bit Number	Bit Mnemonic	Description
7	GPE7_FUN_SLT2	Set GPIOE7 complex function 2 Refer to GPIOE_FUN, p. 49
6	GPE6_FUN_SLT2	Set GPIOE6 complex function 2 Refer to GPIOE_FUN, p. 49
5	GPE5_FUN_SLT2	Set GPIOE5 complex function 2 Refer to GPIOE_FUN, p. 49
4	GPE4_FUN_SLT2	Set GPIOE4 complex function 2 Refer to GPIOE_FUN, p. 49
3-1	Reserved	-
0	GPA0_FUN_SLT2	Set GPIOA0 complex function 2 Refer to GPIOA_FUN2, p. 46

LCD COM pin Setting Table:

COM:

GPIOF0 **(COM0)**
GPIOF1 **(COM1)**
GPIOF2 **(COM2)**
GPIOF3 **(COM3)**

COM	Register Setting
COM0	0x2D of bit 0: GPF0_FUN_SLT = 1
COM1	0x2D of bit 3-2: GPF1_FUN_SLT[1:0] = 01
COM2	0x2D of bit 4: GPF2_FUN_SLT = 1
COM3	0x2D of bit 6: GPF3_FUN_SLT = 1

LCD SEG pin Setting Table:

SEG:

GPIOB5 ~ B0 **(SEG31 ~ SEG26)**
GPIOC7 ~ C3 **(SEG25 ~ SEG21)**
GPIOD7 ~ D0 **(SEG20 ~ SEG13)**
GPIOE7 ~ E0 **(SEG12 ~ SEG5)**
GPIOF7 ~ F5 **(SEG4 ~ SEG2)**
GPIOG7 ~ G6 **(SEG1 ~ SEG0)**

ACOM	Register Setting	BCOM	Register Setting
SEG31	0x29 of bit 3: GPB5_FUN_SLT = 1	SEG15	0x2B of bit 1: GPD2_FUN_SLT = 1
SEG30	0x29 of bit 2: GPB4_FUN_SLT = 1	SEG14	0x2B of bit 1: GPD1_FUN_SLT = 1
SEG29	0x29 of bit 1: GPB3_FUN_SLT = 1	SEG13	0x2B of bit 1: GPD0_FUN_SLT = 1
SEG28	0x29 of bit 0: GPB2_FUN_SLT = 1	SEG12	0x2B of bit 1: GPE7_FUN_SLT = 1
SEG27	0x2A of bit 7: GPB1_FUN_SLT = 1	SEG11	0x2B of bit 0: GPE6_FUN_SLT = 1
SEG26	0x2A of bit 6: GPB0_FUN_SLT = 1	SEG10	0x2C of bit 6: GPE5_FUN_SLT = 1
SEG25	0x2A of bit 5: GPC7_FUN_SLT = 1	SEG9	0x2C of bit 4: GPE4_FUN_SLT = 1
SEG24	0x2A of bit 4: GPC6_FUN_SLT = 1	SEG8	0x2C of bit 2: GPE3_FUN_SLT = 1
SEG23	0x2A of bit 3: GPC5_FUN_SLT = 1	SEG7	0x2E of bit 7: GPE2_FUN_SLT = 1
SEG22	0x2A of bit 2: GPC4_FUN_SLT = 1	SEG6	0x2E of bit 6: GPE1_FUN_SLT = 1
SEG21	0x2A of bit 1: GPC3_FUN_SLT = 1	SEG5	0x2E of bit 5: GPE0_FUN_SLT = 1
SEG20	0x2A of bit 0: GPD7_FUN_SLT = 1	SEG4	0x2E of bit 4: GPF7_FUN_SLT = 1
SEG19	0x2A of bit 0: GPD6_FUN_SLT = 1	SEG3	0x2E of bit 3: GPF6_FUN_SLT = 1
SEG18	0x2A of bit 0: GPD5_FUN_SLT = 1	SEG2	0x2E of bit 2: GPF5_FUN_SLT = 1
SEG17	0x2A of bit 0: GPD4_FUN_SLT = 1	SEG1	0x2E of bit 1: GPG7_FUN_SLT = 1
SEG16	0x2A of bit 0: GPD3_FUN_SLT = 1	SEG0	0x2E of bit 0: GPG6_FUN_SLT = 1

ADC VREF Complex Function Setting Table:

ADC VREF	Register Setting	Shared with GPIO
VREF	GPA2_FUN_SLT[1:0] = 01	GPIOA2

Crystal Oscillator Complex Function Setting Table:

CLKIO	Register Setting	Shared with GPIO
MOSCI1	GPA5_FUN_SLT = 1	GPIOA5
MOSCO1	GPA5_FUN_SLT = 1	GPIOA4
MOSCO2	GPF1_FUN_SLT[1:0] = 10	GPIOF1
MOSCI2	GPF1_FUN_SLT[1:0] = 10	GPIOF0

Notes:

If GPIOA5 = MOSCI1, the complex function of GPIOA4 will be invalid, and auto define GPIOA4 as MOSCO1.
If GPIOF1 = MOSCO2, the complex function of GPIOF0 will be invalid, and auto define GPIOF0 as MOSCI2.

UART Complex Function Setting Table:

UART	Register Setting	Shared with GPIO
RXA	GPA7_FUN_SLT[1:0] = 01	GPIOA0
TXA	GPA7_FUN_SLT[1:0] = 01	GPIOA1
RXB	GPB3_FUN_SLT[1:0] = 10	GPIOE7
TXB	GPB3_FUN_SLT[1:0] = 10	GPIOE6

Notes:

If GPIOA0 = RXA, the complex function of GPIOA1 will be invalid, and auto define GPIOA1 as TXA.
If GPIOE7 = RXB, the complex function of GPIOE6 will be invalid, and auto define GPIOE6 as TXB.

PWM Complex Function Setting Table:

PWM	Register Setting	Shared with GPIO
PWM0A	GPA2_FUN_SLT[1:0] = 10	GPIOA2
PWM0B	GPA3_FUN_SLT = 1	GPIOA3
PWM0C	GPB4_FUN_SLT[1:0] = 10	GPIOB4
PWM1A	GPA1_FUN_SLT[1:0] = 10	GPIOA1
PWM1B	GPB7_FUN_SLT[1:0] = 10	GPIOB7

6.3 Interrupt

The WT56F116S/108S provides total six 8052 Interrupt sources: three 8052 External Interrupts (INT0, INT1, INT3), two Timer/Counter Interrupt (TF0, TF1), and one UART Interrupt (RI0/TI0).

Each of these interrupt sources has its own enable control bit, and can be individually enabled or disabled by setting or clearing the corresponding bit in the Special Function Register IE.

When an interrupt is generated, CPU will jump to interrupt vector from service routine as listed below. If multiple requests of different priority levels are received simultaneously, the request of higher priority level is serviced, and then returned to service routine through RETI instruction. If interrupt flag bit is set, CPU will enter the Interrupt processing again.

Interrupt Vector Table of 8052 & Priority Level Structure:

Keil C Interrupt Number	Interrupt sources	Vector Address	Priority Level (default)	Interrupt Enable Register
0	8052 external interrupt 0	03H	1	IE.0 (EX0)
1	Timer/Counter 0 interrupt	0BH	2	IE.1 (ET0)
2	8052 external interrupt 1	13H	3	IE.2 (EX1)
3	Timer/Counter 1 interrupt	1BH	4	IE.3 (ET1)
4	Serial port 0 interrupt (UART0)	23H	5	IE.4 (ES)
8	8052 external interrupt 3	43H	9	XICON.6 (EX3)

Interrupt Enable register 0

IE0 (8052 interrupt enable register, including INT0/INT1) Address: A8H **Reset value: 00h**

7	6	5	4	3	2	1	0
EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0

Bit Number	Bit Mnemonic	Description
7	EA	1: Enable all interrupt function 0: Disable all interrupt function
6	ES1	1: Enable UART 0 interrupt (WT51F116/108 & WT51F104 are not available) 0: Disable UART 0 interrupt
5	ET2	1: Enable Timer/Counter1 interrupt (WT51F104 is not available) 0: Disable Timer/Counter1 interrupt
4	ES0	1: Enable UART 0 interrupt 0: Disable UART 0 interrupt
3	ET1	1: Enable Timer/Counter1 interrupt 0: Disable Timer/Counter1 interrupt
2	EX1	1: Enable 8052 external interrupt 1 interrupt 0: Disable 8052 external interrupt 1 interrupt
1	ET0	1: Enable Timer/Counter0 interrupt 0: Disable Timer/Counter0 interrupt
0	EX0	1: Enable 8052 external interrupt 0 interrupt 0: Disable 8052 external interrupt 0 interrupt

Interrupt Enable register 1

XICON (8052 INT3 interrupt enable register) Address: C0H **Reset value: 00h**

7	6	5	4	3	2	1	0
PX3	EX3	IE3	-	-	-	-	-

Bit Number	Bit Mnemonic	Description
7	PX3	Define the interrupt priority of external interrupt 3 1: INT3 has the higher priority 0: INT3 has no higher priority
6	EX3	1: Enable external interrupt 3 interrupt 0: Disable external interrupt 3 interrupt
5	IE3	If CPU detects external interrupt 3 interrupt, IE3 will be cleared by hardware. 1: has external interrupt 3 request 0: no external interrupt 3 request
4-0	Reserved	-

- : unimplemented

Interrupt priority register

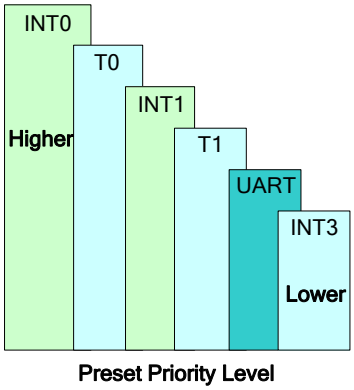
IP (8052 interrupt priority register) Address: B8H **Reset value: 00h**

7	6	5	4	3	2	1	0
-	-	-	PS	PT1	PX1	PT0	PX0

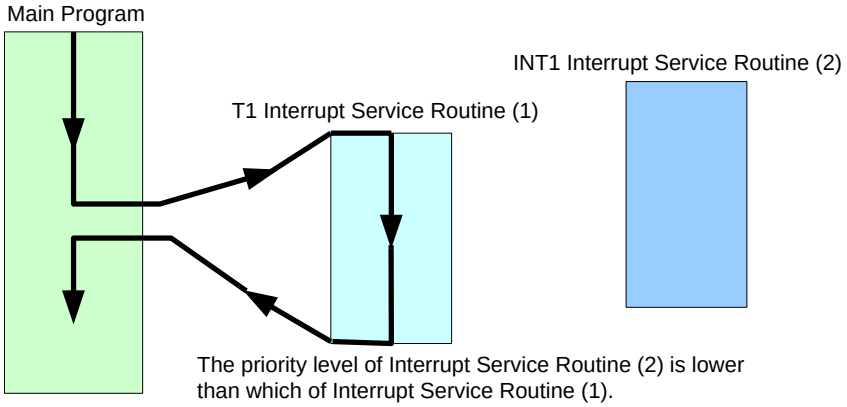
Bit number	Bit Mnemonic	Description
7-5	Reserved	-
4	PS	Define the interrupt priority of UART 0 1: has the higher priority 0: has the lower priority
3	PT1	Define the interrupt priority of Timer/Counter 1 1: has the higher priority 0: has the lower priority
2	PX1	Define the interrupt priority of external interrupt 1 1: has the higher priority 0: has the lower priority
1	PT0	Define the interrupt priority of Timer/Counter 0 1: has the higher priority 0: has the lower priority
0	PX0	Define the interrupt priority of external interrupt 0 1: has the higher priority 0: has the lower priority

-: unimplemented

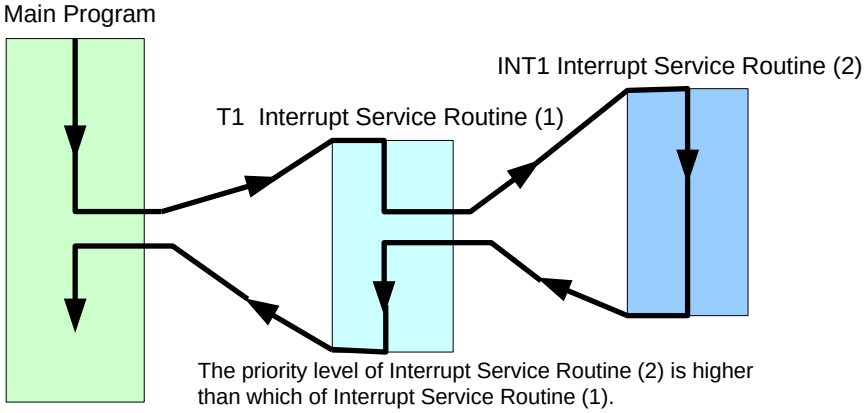
As illustrated below, if not set the priority level in Interrupt Priority Register (IP), the priority level of interrupt will be: **INT0 > T0 > INT1 > T1 > UART > INT3.**



If the higher priority is assigned to any one of the interrupts, such as set PT1 = 1, then the priority level will be: **T1 > INT0 > T0 > INT1 > UART0 > INT3.**



If PT1 = 1 and PX1 = 1, then the priority level will be: **INT1 > T1 > INT0 > T0 > UART0 > INT3**, and so on. The figure below illustrated the executing procedures under different priority levels.

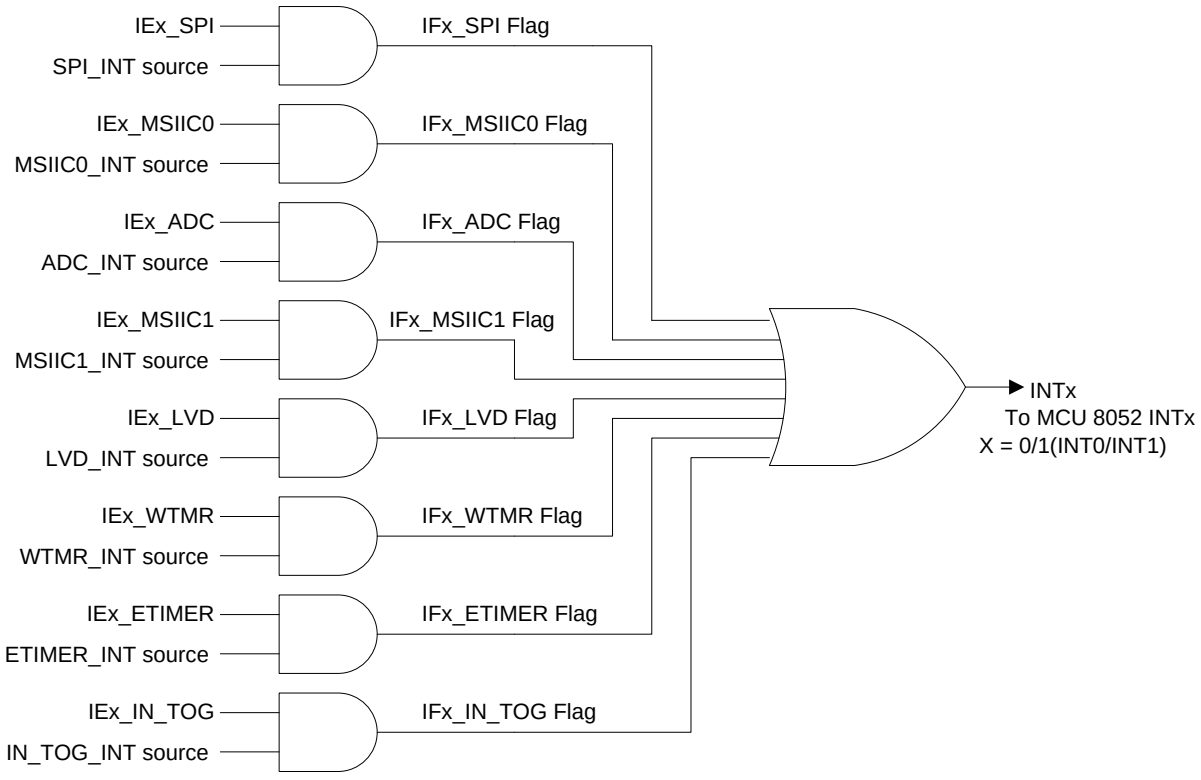


6.3.1 8052 External Interrupt 0/1

The WT56F116S/108S supports eight peripheral interrupt sources which are derived from 8052 external interrupt 0/1, as described below.

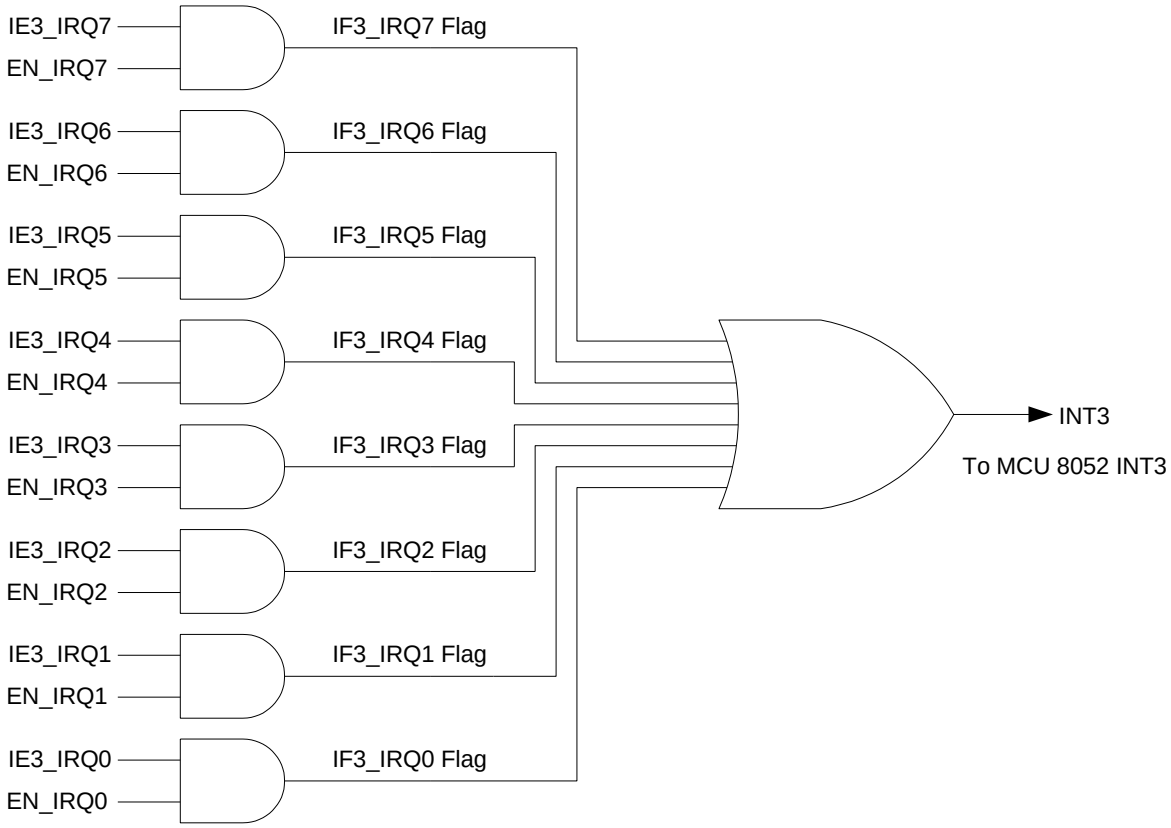
1. SPI interrupt
2. The 0th I2C Interrupt
3. ADC interrupt
4. The 1st I2C Interrupt
5. LVD interrupt
6. Watch Timer Interrupt
7. Enhanced Timer/Counter interrupt
8. General-purpose I/O port input triggered interrupt

The figure below shows the interrupt sources of 8052 external interrupt 0/1:



6.3.2 8052 External Interrupt 3

WT56F116S/108S contains 8 External Interrupt Request input pins. An interrupt is generated by using 8052 External Interrupt Vector 3, as illustrated below (refer to section 6.5 for more details).



8052 External Interrupt 0 Control Register IE0_CTL (XFR: 0x30) **Reset value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	IE0_SPI	IE0_MSIIC0	IE0_ADC	IE0_MSIIC1	IE0_LVD	IE0_WTMR	IE0_ETIMER	IE0_IN_TOG

Bit Number	Bit Mnemonic	Description
7	IE0_SPI	1: Enable SPI Interrupt generated by INT0 0: Disable SPI Interrupt generated by INT0
6	IE0_MSIIC0	1: Enable the 0th M/S IIC Interrupt generated by INT0 0: Disable the 0th M/S IIC Interrupt generated by INT0
5	IE0_ADC	1: Enable ADC Interrupt generated by INT0 0: Disable ADC Interrupt generated by INT0
4	IE0_MSIIC1	1: Enable the 1st M/S IIC Interrupt generated by INT0 0: Disable the 1st M/S IIC Interrupt generated by INT0
3	IE0_LVD	1: Enable LVD Interrupt generated by INT0 0: Disable LVD Interrupt generated by INT0
2	IE0_WTMR	1: Enable Watch Timer Interrupt generated by INT0 0: Disable Watch Timer Interrupt generated by INT0
1	IE0_ETIMER	1: Enable Enhanced Timer Interrupt generated by INT0 0: Disable Enhanced Timer Interrupt generated by INT0
0	IE0_IN_TOG	1: Enable All-Input Toggle Interrupt generated by INT0 0: Disable All-Input Toggle Interrupt generated by INT0 GPIO are the 16 GPIOs listed by Registers 0x60 and 0x61.

- **: unimplemented**

8052 External Interrupt 1 Control Register IE1_CTL (XFR: 0x31) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	IE1_SPI	IE1_MSIIC0	IE1_ADC	IE1_MSIIC1	IE1_LVD	IE1_WTMR	IE1_ETIMER	IE1_IN_TOG

Bit Number	Bit Mnemonic	Description
7	IE1_SPI	1: Enable SPI Interrupt generated by INT1 0: Disable SPI Interrupt generated by INT1
6	IE1_MSIIC0	1: Enable the 0th M/S IIC Interrupt generated by INT1 0: Disable the 0th M/S IIC Interrupt generated by INT1
5	IE1_ADC	1: Enable ADC Interrupt generated by INT1 0: Disable ADC Interrupt generated by INT1
4	IE1_MSIIC1	1: Enable the 1st M/S IIC Interrupt generated by INT1 0: Disable the 1st M/S IIC Interrupt generated by INT1
3	IE1_LVD	1: Enable LVD Interrupt generated by INT1 0: Disable LVD Interrupt generated by INT1
2	IE1_WTMR	1: Enable Watch Timer Interrupt generated by INT1 0: Disable Watch Timer Interrupt generated by INT1
1	IE1_ETIMER	1: Enable Enhanced Timer Interrupt generated by INT1 0: Disable Enhanced Timer Interrupt generated by INT1

Bit Number	Bit Mnemonic	Description
0	IE1_IN_TOG	1: Enable All-Input Toggle Interrupt generated by INT1 0: Disable All-Input Toggle Interrupt generated by INT1 GPIO are the 16 GPIOs listed by Registers 0x60 and 0x61.

- **: unimplemented**

8052 External Interrupt 3 Control Register INT3_IRQ [7:0] (XFR: 0x34) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	IE3_IRQ[7:0]							

Bit Number	Bit Mnemonic	Description
7	IE3_IRQ7	1: Enable IRQ7 Interrupt generated by INT3 0: Disable IRQ7 Interrupt generated by INT3
6	IE3_IRQ6	1: Enable IRQ6 Interrupt generated by INT3 0: Disable IRQ6 Interrupt generated by INT3
5	IE3_IRQ5	1: Enable IRQ5 Interrupt generated by INT3 0: Disable IRQ5 Interrupt generated by INT3
4	IE3_IRQ4	1: Enable IRQ4 Interrupt generated by INT3 0: Disable IRQ4 Interrupt generated by INT3
3	IE3_IRQ3	1: Enable IRQ3 Interrupt generated by INT3 0: Disable IRQ3 Interrupt generated by INT3
2	IE3_IRQ2	1: Enable IRQ2 Interrupt generated by INT3 0: Disable IRQ2 Interrupt generated by INT3
1	IE3_IRQ1	1: Enable IRQ1 Interrupt generated by INT3 0: Disable IRQ1 Interrupt generated by INT3
0	IE3_IRQ0	1: Enable IRQ0 Interrupt generated by INT3 0: Disable IRQ0 Interrupt generated by INT3

8052 External Interrupt 0 (INT0) Flag Register IF0_FLAG (XFR: 0x35) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	IF0_SPI	IF0_MSIIC0	IF0_ADC	IF0_MSIIC1	IF0_LVD	IF0_WTMR	IF0_ETIMER	IF0_IN_TOG

Bit Number	Bit Mnemonic	Description
7	IF0_SPI	1: SPI Interrupt Event Flag be set, SPI Interrupt Flag Clear, refer to section 6.12 XFR[0xC3]
6	IF0_MSIIC0	1: the 0th M/S IIC Interrupt Event Flag be set
5	IF0_ADC	1: ADC Interrupt Event Flag be set, will be cleared automatically after ADC conversion
4	IF0_MSIIC1	1: the 1st M/S IIC Interrupt Event Flag be set
3	IF0_LVD	1: LVD Interrupt Event Flag be set, LVD Interrupt Flag Clear, refer to section 5.7 XFR[0x03]
2	IF0_WTMR	1: Watch Timer Interrupt Event Flag be set, Watch Timer Interrupt Flag Clear, refer to section 6.9 XFR[0x7C]

Bit Number	Bit Mnemonic	Description
1	IF0_ETIMER	1: Enhanced Timer Interrupt Event Flag be set, Enhanced Timer Interrupt Flag Clear, refer to section 6.12 XFR[0xB2]
0	IF0_IN_TOG	1: All-Input Toggle Interrupt Event Flag be set, Input Toggle Interrupt Flag Clear, refer to section 6.7 XFR[0x6A]

- **: unimplemented**

8052 External Interrupt 1 (INT1) Flag Register IF1_FLAG (XFR: 0x36) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	IF1_SPI	IF1_MSIIC0	IF0_MSIIC0	IF1_MSIIC1	IF1_LVD	IF1_WTMR	IF1_ETIMER	IF1_IN_TOG

Bit Number	Bit Mnemonic	Description
7	IF1_SPI	1: SPI Interrupt Event Flag be set, SPI Interrupt Flag Clear, refer to section 6.12 XFR[0xC3]
6	IF1_MSIIC0	1: the 1st M/S IIC Interrupt Event Flag be set
5	IF1_ADC	1: ADC Interrupt Event Flag be set, will be cleared automatically after ADC conversion
4	IF1_MSIIC1	1: the 1st M/S IIC Interrupt Event Flag be set
3	IF1_LVD	1: LVD Interrupt Event Flag be set, LVD Interrupt Flag Clear, refer to section 5.7 XFR[0x03]
2	IF1_WTMR	1: Watch Timer Interrupt Event Flag be set, Watch Timer Interrupt Flag Clear, refer to section 6.9 XFR[0x7C]
1	IF1_ETIMER	1: Enhanced Timer Interrupt Event Flag be set, Enhanced Timer Interrupt Flag Clear, refer to section 6.12 XFR[0xB2]
0	IF1_IN_TOG	1: All-Input Toggle Interrupt Event Flag be set, Input Toggle Interrupt Flag Clear, refer to section 6.7 XFR[0x6A]

- **: unimplemented**

8052 External Interrupt 3 (INT3) Flag Register IF3_IRQ [7:0] (XFR: 0x39) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	IF3_IRQ[7:0]							

Bit Number	Bit Mnemonic	Description
7	IF3_IRQ7	1: IRQ7 Interrupt Event Flag be set, IRQ Interrupt Flag Clear, refer to section 6.5 XFR[0x42]
6	IF3_IRQ6	1: IRQ6 Interrupt Event Flag be set, IRQ Interrupt Flag Clear, refer to section 6.5 XFR[0x42]
5	IF3_IRQ5	1: IRQ5 Interrupt Event Flag be set, IRQ Interrupt Flag Clear, refer to section 6.5 XFR[0x42]
4	IF3_IRQ4	1: IRQ4 Interrupt Event Flag be set, IRQ Interrupt Flag Clear, refer to section 6.5 XFR[0x42]
3	IF3_IRQ3	1: IRQ3 Interrupt Event Flag be set, IRQ Interrupt Flag Clear, refer to section 6.5 XFR[0x42]

Bit Number	Bit Mnemonic	Description
2	IF3_IRQ2	1: IRQ2 Interrupt Event Flag be set, IRQ Interrupt Flag Clear, refer to section 6.5 XFR[0x42]
1	IF3_IRQ1	1: IRQ1 Interrupt Event Flag be set, IRQ Interrupt Flag Clear, refer to section 6.5 XFR[0x42]
0	IF3_IRQ0	1: IRQ0 Interrupt Event Flag be set, IRQ Interrupt Flag Clear, refer to section 6.5 XFR[0x42]

6.4 Universal Asynchronous Receiver-Transmitter (UART)

The WT56F116S/108S contains two Universal Asynchronous Receiver-Transmitter (UART0 & UART1).

As a standard UART of 8052, the Baud rate is selected by the Serial Baud rate Generator in SFR.

On Transmit and Receive, the SFR SBUF0 uses two separate registers: a transmit buffer and a receive buffer register.

Transmitting data: Writing to SBUF0 register and loads these data in serial output buffer, and starts transmitting.

Receiving data: Reading SBUF0 register and reading the serial receive buffer. The serial port can transmit and receive simultaneously. It is also one byte receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the receive register to prevent data loss.

The peripheral registers of UART:

SFR Name	Address	Description
PCON	87H	8052 Power Control Register
SCON0	98H	Serial Port 0, Control Register
SBUF0	99H	Serial Port 0, Data Buffer
SBRG0H	9AH	Serial Baud Rate Generator 0, high byte
SBRG0L	9BH	Serial Baud Rate Generator 0, low byte
SCON1	D8H	Serial Port 1, Control Register
SBUF1	D9H	Serial Port 1, Data Buffer
SBRG1H	DAH	Serial Baud Rate Generator 1, high byte
SBRG1L	DBH	Serial Baud Rate Generator 1, low byte

UART0 Peripheral Registers

PCON (8052 Power Control Register) Address: 87H

7	6	5	4	3	2	1	0
SMOD1	-	-	-	-	-	-	-

SMOD1: UART0 dual rate bit.

-: unimplemented.

SBUF0 (8052 UART0 buffer) Address: 99H

7	6	5	4	3	2	1	0
SBUF0.7	SBUF0.6	SBUF0.5	SBUF0.4	SBUF0.3	SBUF0.2	SBUF0.1	SBUF0.0

The Serial Data Buffer of UART0. It is used to hold the bytes to be received or the bytes to be transmitted from UART0.

SBRG0H: Address: 9Ah

7	6	5	4	3	2	1	0
SBRG_EN	BRG_M[10]	BRG_M[9]	BRG_M[8]	BRG_M[7]	BRG_M[6]	BRG_M[5]	BRG_M[4]

Used to configure the Baud rate of UART0 and it must be accessed together with SBRG0L.

SBRG0L: Address: 9Bh

7	6	5	4	3	2	1	0
BRG_M[3]	BRG_M[2]	BRG_M[1]	BRG_M[0]	BRG_F[3]	BRG_F[2]	BRG_F[1]	BRG_F[0]

Used to configure the Baud rate of UART0 and it must be accessed together with SBRG0H.

SCON0 (8052 UART0 Control Register) Address: 98H

7	6	5	4	3	2	1	0
SM0_1	SM0_2	SM0_3	REN_0	TB8_0	RB8_0	TI_0	RI_0

Bit Number	Bit Mnemonic	Description
7-6	SM0_1, SM0_2	UART0 mode selection 00: Mode 0 01: Mode 1 10: Mode 2 11: Mode 3
5	SM0_3	Multi-processor Communication Enable bit In Mode 0, if SM0_3 = 0, the multi-processor communication function is disabled. In Mode 1, 2, or 3, if SM0_3 = 1, the multi-processor communication function is enabled.
4	REN_0	UART Receive Enable bit must be cleared by software. REN_0 = 1, receive starts. REN_0 = 0, receive stops.
3	TB8_0	The 9th transmit bit in Mode 2 or Mode 3, can be set or cleared by software.
2	RB8_0	In Mode 0, this bit is invalid. In Mode 1, this bit is Stop bit if SM0_3 = 0 In Mode 2 or 3, the 9th data bit that was received.
1	TI_0	Transmit Interrupt Flag. When an interrupt is complete, this bit will not be restored to “0”, and it must be cleared by software. In Mode 0, this bit is set by hardware at the end of the 8th bit, and meantime it can commence a TI_0 interrupt. In Mode 1, 2, or 3, this bit is set by hardware at the end of transmitting Stop bit, and meantime it can commence a TI_0 interrupt.
0	RI_0	Receive Interrupt Flag. When an interrupt is complete, this bit will not be restored to “0”, and it must be cleared by software. In Mode 0, this bit is set by hardware at the end of the 8th bit, and meantime it can commence a RI_0 interrupt. In Mode 1, 2, or 3, this bit is set by hardware at the end of transmitting Stop bit, and meantime it can commence a RI_0 interrupt.

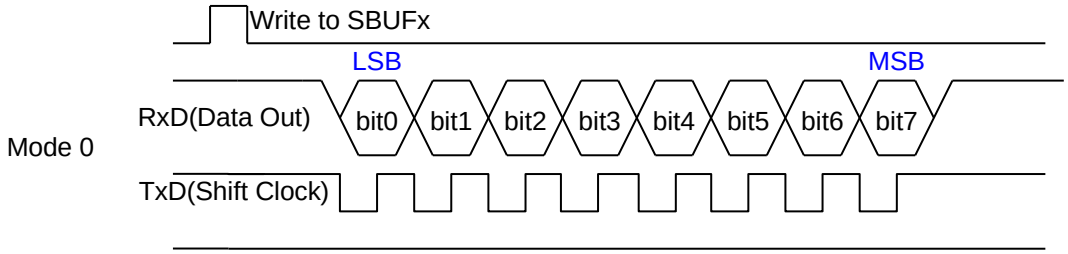
The Serial Interface 0 can operate in four modes, as described below.

SM0_1	SM0_2	Mode	Function	Baud Rate
0	0	0	Shift Register	Fosc/12
0	1	1	8-bit UART	Software programmed
1	0	2	8-bit UART	Fosc/32 or Fosc/64
1	1	3	9-bit UART	Software programmed

***Fosc = MCU clock**

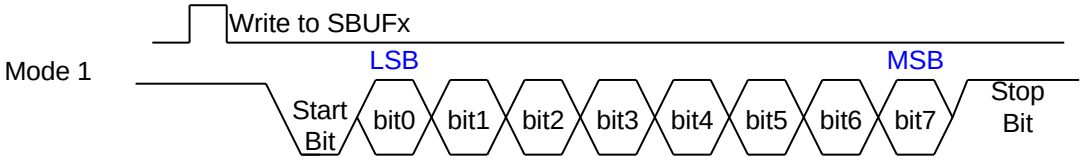
Mode 0

In Mode 0, the Baud rate of Shift transmission register is fixed at 1/12 of the oscillator frequency (*fOSC*/12). At 12 MHz, the Baud rate is 1Mbps. In this mode, no matter on receive or transmit data, Rx0 of CPUs connects each other worked as a serial data bus and Tx0 connects each other worked as a Shift pulse. On Receive, Tx0 pin sent out the shift pulse, and the serial data is received by Rx0 pin; On Transmit, it is also based on the shift pulse sent by Tx0 pin, and sent the serial data by Rx0 pin.



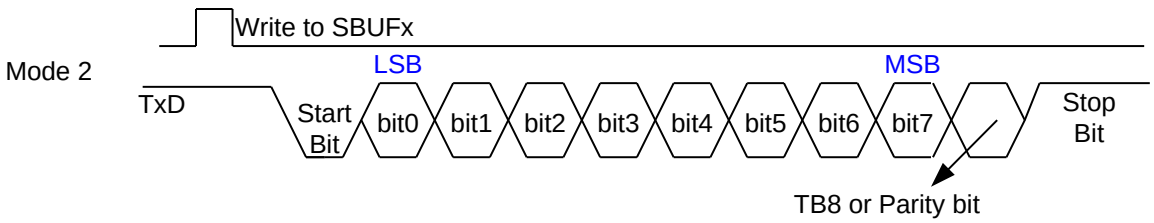
Mode 1

Mode 1 may have a variable Baud rate for serial data transmit, and the Baud rate is controlled by Timer 1.
In this mode, the Rx0 pin of WT56F116S/108S connects to the destination TxD pin, and the Tx0 pin of WT56F116S/108S connects to the destination RxD pin.
10 bits are length of transmitted or received: a Start bit, 8 data bits, and a Stop bit. The first bit is the low level start bit (0), followed by the 8 data bits (LSB first, starts from bit 0), then the high level stop bit (1) after bit 7 (MSB).



Mode 2

Mode 2 operates at *fOSC*/32 (SMOD = 1) or *fOSC*/64 (SMOD = 0) for serial data transmission. As for the wire connection, Rx0 pin of WT56F116S/108S connects to destination TxD pin and Tx0 pin of WT56F116S/108S connects to destination RxD pin. 11 bits are length of transmitted or received: a Start bit, 8 data bits, a Parity bit, and 1 Stop bit. The first bit is the low level start bit (0), followed by the 8 data bits (LSB first, starts from bit 0), then the Parity bit after bit 7, and finally the high level stop bit.
On Transmit, TB8_0 in SCON0 is the 9th data bit. The TB8_0 in SCON0 will transmit the 9th data bit; On Receive, the RB8_0 in SCON0 will receive the 9th data bit.



Mode 3

The Baud rate in mode 3 is variable for serial data transmission, and it is controlled by Timer 1. The operation in Mode 3 is the same as Mode 2.

Serial Baud rate of UART0:

SBRG_EN (SBRG0H.7)	SMOD1 (PCON.7)	Baud Rate for UART0
0	0	$\frac{1}{32}\times\frac{f_{osc}}{12\times(256-TH1)}$
0	1	$\frac{1}{16}\times\frac{f_{osc}}{12\times(256-TH1)}$
1	0	$\frac{f_{osc}}{32*(BRG\_M[10:0]+\frac{BRG\_F[3:0]}{16})}$
1	1	$\frac{f_{osc}}{16*(BRG\_M[10:0]+\frac{BRG\_F[3:0]}{16})}$

If SBRG_EN (SBRG0H.7) = 1& SMOD1(PCON.7) = 1

UART0 Baud rate = $\frac{f_{osc}}{16*(BRG\_M[10:0]+\frac{BRG\_F[3:0]}{16})}$

Baud rate supporting table:

	12 MHz				
Bits/sec	**Baud Rate Register**	**BRG_M**	**BRG_F**	**Actual**	**Error**
600	1250	1250	0	600	0.0%
1200	625	625	0	1200	0.0%
2400	312.5	312	8	2400	0.0%
4800	156.25	156	4	4800	0.0%
9600	78.125	78	2	9600	0.0%
14400	52.083	52	1	14405	0.04%
19200	39.0625	39	1	19200	0.0%
38400	19.531	19	8	38461	0.16%
57600	13	13	0	57692	0.16%
115200	6.5	6	8	115384	0.16%
230400	3.25	3	4	230769	0.16%

UART1 Peripheral Registers

SBUF1 (8052 UART1 buffer) Address: D9H

7	6	5	4	3	2	1	0
SBUF1.7	SBUF1.6	SBUF1.5	SBUF1.4	SBUF1.3	SBUF1.2	SBUF1.1	SBUF1.0

The Serial Data Buffer of UART1. It is used to hold the bytes to be received or the bytes to be transmitted from UART1.

SBRG1H: Address: DAh

7	6	5	4	3	2	1	0
SBRG1_EN	BRG1_M[10]	BRG1_M[9]	BRG1_M[8]	BRG1_M[7]	BRG1_M[6]	BRG1_M[5]	BRG1_M[4]

Used to configure the Baud rate of UART1 and it must be accessed together with SBRG1L.

SBRG1L: Address: DBh

7	6	5	4	3	2	1	0
BRG1_M[3]	BRG1_M[2]	BRG1_M[1]	BRG1_M[0]	BRG1_F[3]	BRG1_F[2]	BRG1_F[1]	BRG1_F[0]

Used to configure the Baud rate of UART1 and it must be accessed together with SBRG1H.

SCON1 (8052 UART1 Control Register) Address: D8H

7	6	5	4	3	2	1	0
SM1_1	SM1_2	SM1_3	REN_1	TB8_1	RB8_1	TI_1	RI_1

UART1 Control Register.

Bit Number	Bit Mnemonic	Description
7-6	SM1_1, SM1_2	UART0 mode selection 00: Mode 0 01: Mode 1 10: Mode 2 11: Mode 3
5	SM1_3	Multi-processor Communication Enable bit In Mode 0, if SM0_3 = 0, the multi-processor communication function is disabled. In Mode 1, 2, or 3, if SM0_3 = 1, the multi-processor communication function is enabled.
4	REN_1	UART Receive Enable bit must be cleared by software. REN_1 = 1, receive starts. REN_1 = 0, receive stops.
3	TB8_1	The 9th transmit bit in Mode 2 or Mode 3, can be set or cleared by software.
2	RB8_1	In Mode 0, this bit is invalid. In Mode 1, this bit is Stop bit if SM0_3 = 0 In Mode 2 or 3, the 9th data bit that was received.
1	TI_1	Transmit Interrupt Flag. When an interrupt is complete, this bit will not be restored to “0”, and it must be cleared by software. In Mode 0, this bit is set by hardware at the end of the 8th bit, and meantime it can commence a TI_1 interrupt. In Mode 1, 2, or 3, this bit is set by hardware at the end of transmitting Stop bit, and meantime it can commence a TI_1 interrupt.
0	RI_1	Receive Interrupt Flag. When an interrupt is complete, this bit will not

Bit Number	Bit Mnemonic	Description
		be restored to “0”, and it must be cleared by software. In Mode 0, this bit is set by hardware at the end of the 8th bit, and meantime it can commence a RI_1 interrupt. In Mode 1, 2, or 3, this bit is set by hardware at the end of transmitting Stop bit, and meantime it can commence a RI_0 interrupt.

The Serial Interface 1 can operate in four modes, as described below.

SM1_1	SM1_2	Mode	Function	Baud Rate
0	0	0	Shift Register	Fosc/12
0	1	1	8-bit UART	Software programmed
1	0	2	8-bit UART	Fosc/32 or Fosc/64
1	1	3	9-bit UART	Software programmed

***Fosc = MCU clock**

4 modes of UART1, please refer to the previous section UART0.

Serial Baud rate of UART1:

SBRG1_EN (SBRG1H.7)	SMOD2 (PCON.6)	Baud Rate for UART1
0	0	$\frac{1}{32}\times\frac{f_{osc}}{12\times(65536-RCAP2)}$
0	1	$\frac{1}{16}\times\frac{f_{osc}}{12\times(65536-RCAP2)}$
1	X	$\frac{f_{osc}}{16*(BRG\_M[10:0]+\frac{BRG\_F[3:0]}{16})}$

If SBRG1_EN (SBRG1H.7) = 1

UART0 Baud rate = $\frac{f_{osc}}{16*(BRG\_M[10:0]+\frac{BRG\_F[3:0]}{16})}$

Baud rate supporting table:

	12 MHz				
Bits/sec	**Baud Rate Register**	**BRG_M**	**BRG_F**	**Actual**	**Error**
600	1250	1250	0	600	0.0%
1200	625	625	0	1200	0.0%
2400	312.5	312	8	2400	0.0%
4800	156.25	156	4	4800	0.0%
9600	78.125	78	2	9600	0.0%
14400	52.083	52	1	14405	0.04%
19200	39.0625	39	1	19200	0.0%
38400	19.531	19	8	38461	0.16%
57600	13	13	0	57692	0.16%
115200	6.5	6	8	115384	0.16%
230400	3.25	3	4	230769	0.16%

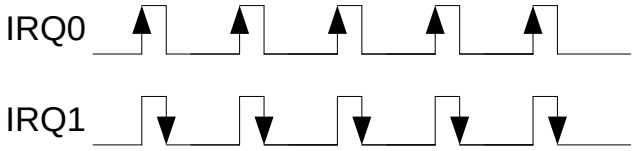
WT56F116S/108S supports one UART; the UART can select different RX/TX path to prevent the pin being occupied.

UART	**Register Setting**	**Input/output pin**
RXA	XFR: 0x25 GPA7_FUN_SLT[1:0] = 01	GPIOA7
TXA		GPIOA6
RXB	XFR: 0x28 GPB3_FUN_SLT[1:0] = 10	GPIOB3
TXB		GPIOB2

6.5 External Interrupt Request (IRQ)

- Supports 8 input Interrupts and built-in digital Filter. (The clock source of digital filer is internal oscillator 12 MHz)
- Supports single-side positive edge-triggered, negative edge-triggered, or positive edge and negative edge triggered simultaneously

Single side triggered:



Bidirectional triggered:

External Interrupt Request (IRQ) Control Register EN_IRQ [7:0] (XFR: 0x40) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	EN_IRQ[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	EN_IRQ[7:0]	External Interrupt Request Enable setting. Each bit is corresponded to the related IRQ pin. 1: Enable the External Interrupt Request of the corresponding pins 0: Disable the External Interrupt Request of the corresponding pins

External Interrupt Request (IRQ) Status Register EVT_IRQ [7:0] (XFR: 0x41) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	EVT_IRQ[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	EVT_IRQ[7:0]	External Interrupt Request Status. Each bit is corresponded to the related IRQ status. 1: an interrupt trigger occurred in the corresponding pins. 0: an interrupt trigger not occurred in the corresponding pins.

External Interrupt Request (IRQ) Clear Register CLR_IRQ [7:0] (XFR: 0x42) Reset Value: 00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	CLR_IRQ[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	CLR_IRQ[7:0]	External Interrupt Request Clear 1: writing one to the corresponding bits can clear the interrupt status 0: no action

External Interrupt Request (IRQ) Bi-directional Trigger Register IRQ_CHG [7:0] (XFR: 0x43) Reset Value: 00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	IRQ_CHG[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	IRQ_CHG[7:0]	External Interrupt Request Trigger setting 1: Bi-directional triggered 0: Single-side triggered (work together with IRQ_EDGE[7:0] to set positive or negative triggered)

External Interrupt Request (IRQ) Trigger Edge Register IRQ_EDGE [7:0] (XFR: 0x44) Reset Value: 00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	IRQ_EDGE[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	IRQ_EDGE[7:0]	External Interrupt Request Trigger Edge setting 1: negative edge triggered 0: positive edge triggered

6.6 Pulse Width Modulation (PWM)

WT56F116S/108S provides two 16-bit precise Pulse Width Modulation modules to generate periods and Duty cycles.

- Output Frequency is 65535 levels; frequency range: 6 MHz ~ 183.1 Hz (at IRC 12 MHz)
- The resolutions of Duty and period and Source clock are closely related to each other.

$$\text{Source clock} = 2^{\text{Duty resolution}} \times \text{Period}$$

For example, if Source clock is IRC 12 MHz, Duty Resolution is 10 bits, then the period range is limited within 11.7 kHz.

- Output type: push pull or open drain, can be configured by GPIOx_TYP[x] (GPIOA2, GPIOA3, GPIOB4, GPIOA1, GPIOB7) register.

PWM Control Register PWM_CTL (XFR: 0x50) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	R/W	R/W	-	R/W	R/W	R/W
Name	Reserved		PWM_PLRTY[1:0]		Reserved	LBYTE_UPD_EN	PWM_EN[1:0]	

Bit Number	Bit Mnemonic	Description
7-6	Reserved	-
5-4	PWM_PLRTY[1:0]	Bit 5: 1: PWM1 negative edge output 0: PWM1 positive edge output Bit 4: 1: PWM0 negative edge output 0: PWM0 positive edge output
3	Reserved	-
2	LBYTE_UPD_EN	1: Enable updating PWM output while writing PWM period or Duty Cycle Control Low Bytes Register 0: Disable updating PWM output while writing PWM period or Duty Cycle Control Low Bytes Register
1	PWM_EN[1:0]	1: Enable PWM1 function 0: Disable PWM1 function
0		1: Enable PWM0 function 0: Disable PWM0 function

-: unimplemented.

PWM0 Period Control High Bytes Register PWM0_PRD[15:8] (XFR: 0x51) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM0_PRD[15:8]							

Bit Number	Bit Mnemonic	Description
7-0	PWM0_PRD[15:8]	PWM0_PRD[15:8] sets the output period of PWM0, and which is paired with PWM0_PRD[7:0] to form a 16-bit of period control value. PWM0 period: SOURCE clock/(PWM0_PRD[15:0]+1), source clock: 12 MHz IRC, DC ~ 16 MHz Crystal OSC. 32 kHz IRC and 32.768 kHz Crystal OSC.

PWM0 Period Control Low Bytes Register PWM0_PRD[7:0] (XFR: 0x52) **Reset Value: 01h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM0_PRD[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	PWM0_PRD[7:0]	PWM0_PRD[7:0] sets the output period of PWM0, and which is paired with PWM0_PRD[15:8] to form a 16-bit of period control value. PWM0 period: SOURCE clock/ (PWM0_PRD[15:0]+1), source clock: 12 MHz IRC, DC ~ 16 MHz Crystal OSC. 32 kHz IRC and 32.768 kHz Crystal OSC.

PWM0 Duty Cycle Control High Bytes Register PWM0_DUTY[15:8] (XFR: 0x53) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM0_DUTY[15:8]							

Bit Number	Bit Mnemonic	Description
7-0	PWM0_DUTY[15:8]	Sets the duty cycle output of PWM0. PWM0_DUTY[15:8] sets the duty cycle of PWM0, and is paired with PWM0_DUTY[7:0] to form a 16-bit of duty cycle control value.

Note: The maximum setting of Duty must be a reasonable value.

PWM0 Duty Cycle Control Low Bytes Register PWM0_DUTY[7:0] (XFR: 0x54) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM0_DUTY[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	PWM0_DUTY[7:0]	Set the duty cycle output of PWM0 PWM0_DUTY[7:0] sets the duty cycle of PWM0, and is paired with PWM0_DUTY[15:8] to form a 16-bit of duty cycle control value.

Note: The maximum setting of Duty must be a reasonable value.

PWM1 Period Control High Bytes Register PWM1_PRD[15:8] (XFR: 0x55) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM1_PRD[15:8]							

Bit Number	Bit Mnemonic	Description
7-0	PWM1_PRD[15:8]	PWM1_PRD[15:8] sets the output period of PWM1, and is paired with PWM1_PRD[7:0] to form a 16-bit of duty cycle control value. PWM1 period: SOURCE clock/(PWM1_PRD[15:0]+1), source clock: 12 MHz IRC, DC ~ 16 MHz Crystal OSC. 32 kHz IRC and 32.768 kHz Crystal OSC.

PWM1 Period Control Low Bytes Register PWM1_PRD[7:0] (XFR: 0x56) **Reset Value: 01h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM1_PRD[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	PWM1_PRD[7:0]	PWM1_PRD[7:0] sets the output period of PWM1, and is paired with PWM1_PRD[15:8] to form a 16-bit of duty cycle control value. PWM1 period: SOURCE clock/(PWM1_PRD[15:0]+1), source clock: 12 MHz IRC, DC ~ 16 MHz Crystal OSC. 32 kHz IRC and 32.768 kHz Crystal OSC.

PWM1 Duty Cycle Control High Bytes Register PWM1_DUTY[15:8] (XFR: 0x57) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM1_DUTY[15:8]							

Bit Number	Bit Mnemonic	Description
7-0	PWM1_DUTY[15:8]	Sets the duty cycle output of PWM1 PWM1_DUTY[15:8] sets the duty cycle of PWM1, and is paired with PWM1_DUTY[7:0] to form a 16-bit of duty cycle control value.

Note: The maximum setting of Duty must be a reasonable value.

PWM1 Duty Cycle Control Low Bytes Register PWM1_DUTY[7:0] (XFR: 0x58) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	PWM1_DUTY[7:0]							

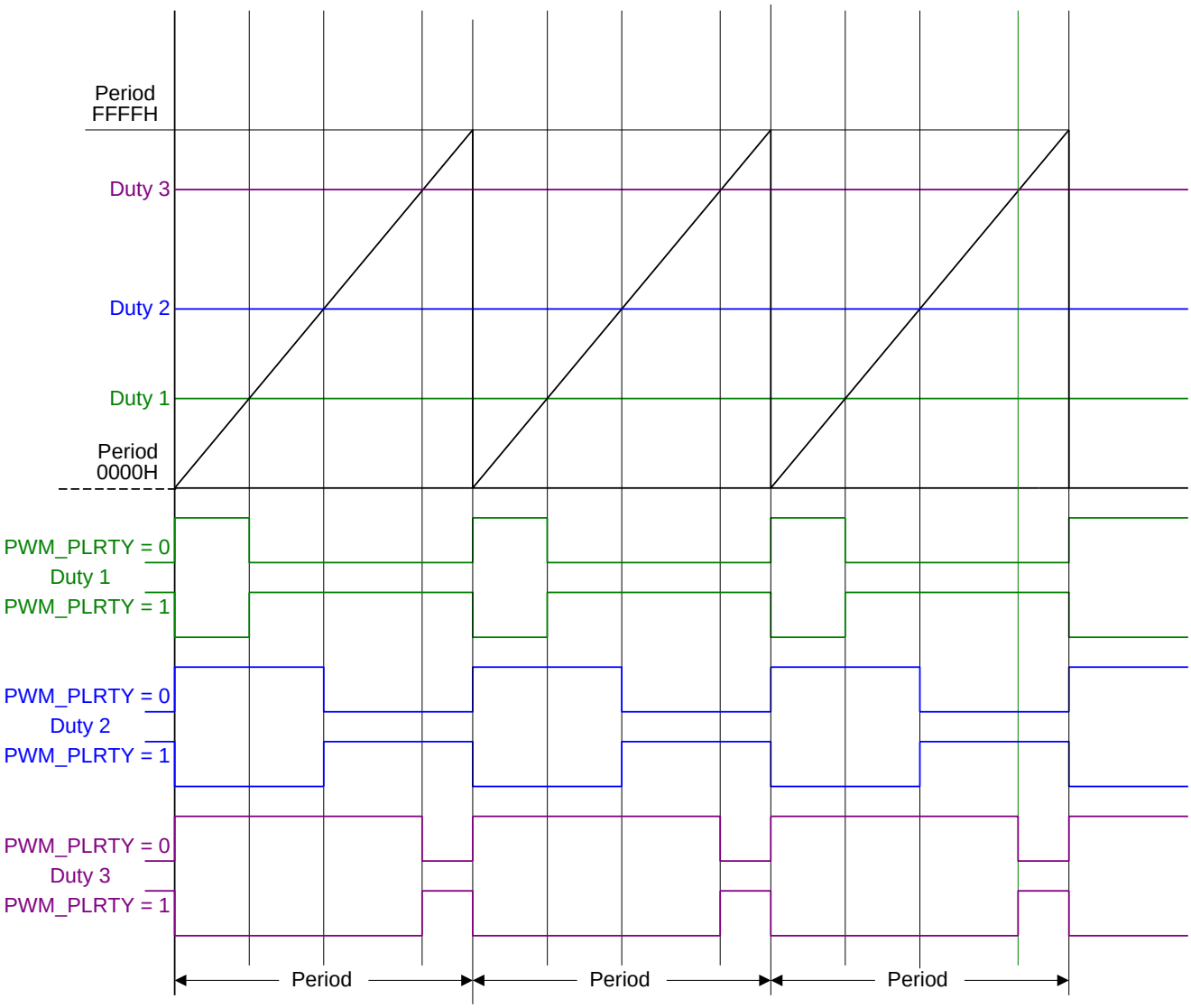
Bit Number	Bit Mnemonic	Description
7-0	PWM1_DUTY[7:0]	Sets the duty cycle of PWM1 PWM1_DUTY[7:0] sets the duty cycle of PWM1, and is paired with PWM1_DUTY[15:8] to form a 16-bit duty cycle control value.

Note: The maximum setting of Duty must be a reasonable value.

PWM0/PWM1 Period Setting example:

$$\text{Period} = \frac{\text{Source clock (if: IRC 12MHz)}}{\text{PWMx\_PRD} + 1}$$

PWMx_PRD	PWM output period
1	6 MHz (Max.)
2	4 MHz
3	3 MHz
11	1 MHz
23	500 kHz
59	200 kHz
119	100 kHz
239	50 kHz
599	20 kHz
1199	10 kHz
2399	5 kHz
2999	4 kHz
3999	3 kHz
5999	2 kHz
11999	1 kHz
23999	500 Hz
29999	400 Hz
39999	300 Hz
59999	200 Hz
65535	183.1 Hz (Min.)



6.7 Power Management

WT56F116S/108S provides four operation modes, as listed below.

- Normal mode
- Green mode
- Idle mode
- Sleep mode

Power Consumption (@ 3V)

	8052	Peripheral Clock	XTAL (high frequency)	XTAL (32768 Hz)	IRC (12 MHz)	IRC (32K)	Power Consumption @3V	Note
Normal 1	on	on	off	off	on	on	1.7 mA	*1
Normal 2	on	on	off	on	on	on	1.7 mA	*2
Normal 3	on	on	on	off	off	on	1.9 mA	*3
Green 1	on	on	off	off	off	on	12 uA	*4*6
Green 2	on	on	off	on	off	off	11 uA	*5*6
Idle 1	off	on	off	off	on	on	500 uA	*7*9*12
Idle 2	off	off	off	off	on	on	350 uA	*8*9*12
Sleep 1	off	off	off	off	off	off	70 uA	*10*12
Sleep 2	off	off	off	off	off	off	5 uA	*11*12
Sleep 3	off	off	off	on	off	off	7.4 uA	*13
Sleep 4	off	off	off	off	off	on	8.2 uA	*14

Notes:

1. LCD power consumption: No Load = 1 uA @3V

2. LVR/LVDR power consumption is abut 6 uA@3V

*1 Normal 1 Mode: MCU all use the internal oscillator, and therefore this mode is the most cost-saving mode, but IRC 12 MHz will be affected by the impact of temperature and supply voltage, please refer to section 7.5.

*2 Normal 2 Mode: use external oscillator 32.768 kHz to calibrate IRC 12 MHz. Calibration can reach ±1%.

*3 Normal 3 Mode: this mode is focused on precise high frequency. Calendar or Clock function can only be achieved by 8052 Timer due to without external oscillator 32.768 kHz.

*4 Green 1 Mode: Source clock select internal IRC 32 kHz, but IRC 32 kHz frequency tolerance is ±30%.

*5 Green 2 Mode: Prior to selecting Source clock of External Crystal Oscillator 32.768 kHz, please manually turn on the power of external crystal oscillator (CRY_12M_PD) to allow external crystal oscillator start oscillation. Due to the external crystal oscillator 32.768 kHz with small frequency tolerance, Canlendar or Clock function can be achieved by Watch Timer.

*6 Prior to switching back to Normal Mode in Green 1 and Green 2 mode, please turn on IRC_12M_PD2 or CRY_12M_PD first, then select Source clock to work at internal IRC 12 MHz or external 12 MHz.

*7 Idle 1 Mode: Enable MCU_CLK_OFF to enter Idle mode, this mode wakeup fast and support the most wakeup sources, please refer to the next page wakeup source illustraiton figure.

*8 Idle 2 Mode: Enable SYSTEM_CLK_OFF to enter Idle mode, this mode turn off Peripheral Clock, thus MCU cannot use INT0/1/_WK to wakeup, please refer to the next page wakeup source illustraiton figure.

*9 Wakeup time of Idle 1 & Idle 2 Mode: Source clock 12 MHz wakeup time 4 * (1/12 MHz) = 333ns; Source clock 32 kHz wakeup time 4 * (1/32 kHz) = 125us

*10 Sleep 1 Mode.: this mode is about Source clock enable IRC12M_CLK_OFF at IRC 12 MHz, allowing MCU to enter Sleep mode, and support fast Wakeup. The wakeup time is start up + 12 * (1/12 MHz) = 1us. Please refer to the figure below.

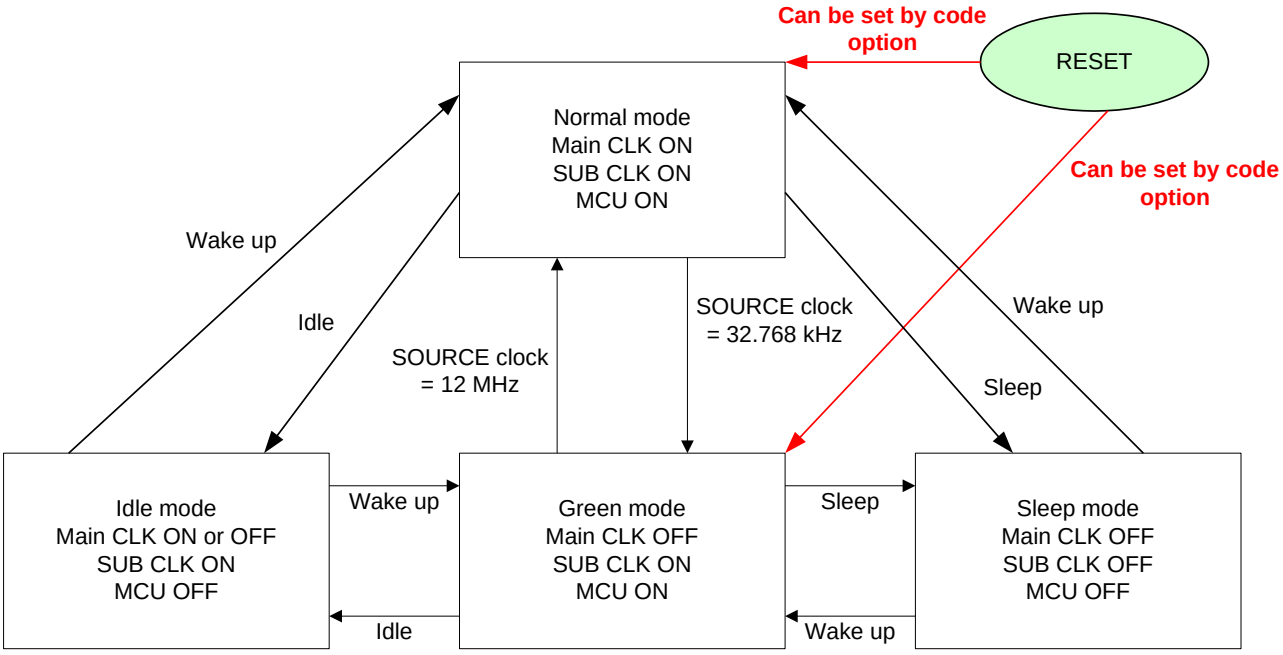
*11 Sleep 2 Mode.: enable SOURCE_CLK_OFF to enter Sleep mode, wakeup time: if Source clock is IRC 12 MHz, start up + 132 * (1/12 MHz) = 21us; if Source clock is external crystal oscillator 12 MHz, 16*1024 * (1/12 MHz) = 1365us. Please refer to the figure below.

*12 Adopts Watch Timer Wakeup in Idle & Sleep mode, turn on the oscillator Power (IRC_32K_PD or CRY_12M_PD) as the clock source of Watch Timer, in the meantime the power-consumption is increasing.

*13 Adopts Watch Timer Wakeup in Sleep mode, and turn on the External crystal oscillator power (CRY_12M_PD) as the clock source of Watch Timer.

*14 Adopts Watch Timer Wakeup in Sleep mode, and turn on the Internal crystal oscillator power (IRC_32K_PD) as the clock source of Watch Timer.

MCU Operation Mode figure:



WT56F116S/108S provides many sources of wakeup returning itself from sleep/idle mode to normal mode.

The figure below illustrated the Wakeup sources below each mode:

		Idle 1	Idle 2	Sleep Mode
SOURCE		MCU_CLK_OFF	SYSTEM_CLK_OFF	SOURCE_CLK_OFF IRC12M_CLK_OFF
NRST		●	●	●
GPIOx_WK[x]		●	●	●
INT0/1_WK	IE0/1_SPI	●		
	IE0/1_MSIIC0	●		
	IE0/1_ADC			
	IE0/1_MSIIC1	●		
	IE0/1_LVD	●	●	●
	IE0/1_WTMR			
	IE0/1_ETIMER	●		
	IE0/1_IN_TOG	●	●	●
INT3_WK	IRQ[7:0]	●		
ADC_WK		●	●	●
WTMR_WK		●	●	●

Notes:

1. ● indicates supporting wakeup
2. GPIOx_WK[x] & IE0/1_IN_TOG: only support 16 General-purpose I/O pin Toggle (GPIOA7、A6、A3、A2、A1、A0、B7、B5、B4、B3、B2、E7、E6、E3、E2、E0)
3. ADC_WK: based on reference source for compare Toggle wakeup
4. WTMR_WK: turn on sub crystal oscillator (IRC 32 kHz or Ext 32 kHz) and sub crystal oscillator power to be the clock source of Watch Timer.

ISP Clock Source Control Register ISP_CHG_CTL (XFR: 0x04) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	-	R/W	R	-	-	-	-
Name	ISP_CHG_12M	Reserved	UART_ISP_CHG	ISP_CHG_FLAG			LVD_RST_ACT_FLG	LVR_ACT_FLG

Bit Number	Bit Mnemonic	Description
7	ISP_CHG_12M	When MCU is in Green & Sleep mode, ISP pin will turn on the internal 12 MHz RC oscillator automatically. 1: Enable 0: Disable
6	Reserved	-
5	UART_ISP_CHG	UART pin (SWUT) trigger ISP clock source as internal 12 MHz RC oscillator. 1: Enable 0: Disable
4	ISP_CHG_FLAG	ISP_CHG_FLAG = 1: MCU has been woken up by SWUT pin. Turn on internal 12 MHz RC oscillator and SOURCE clock switch to 12 MHz. Clear ISP_CHG_FLAG by setting ISP_CHG_12M bit = 0
3-2	Reserved	-
1	LVD_RST_ACT_FLG	Low voltage detection is not connected to the EFT Filter circuit
0	LVR_ACT_FLG	Low voltage reset detection is not connected to the EFT filter circuit

-: unimplemented.

Note: If Source clock is in non-12 MHz application, please add below Forcing Toggle SWUT setting procedure to the program enabling MCU programming repeatedly.

Non 12 MHz mode contains: Green, Sleep mode or use external oscillator (non 12 MHz) can enable ISP_CHG_12M & UART_ISP_CHG bit allow MCU pin trigger to switch the SOURCE clock & ISP clock to internal 12 MHz RC oscillator by SWUT, and meanwhile MCU can receive the correct ISP command.

Mandatory trigger SWUT setting procedures:
1. Program Initialized Enable ISP_CHG_12M & UART_ISP_CHG bit
   rISP_CHG_CTL = 0xA0;
2. Program main loop judge if ISP_CHG_FLAG been triggered, and based on Sleep mode to add one software wakeup mechanism, please refer to the example program.

```
void DRV_CheckSwutTriggerWakeup(void)
{
    //If enable rISP_CHG_CTL of bit 7 and Bit.
    //When Swut pin have hi to low(2V) level, Mcu will change source clock to IRC 12 MHz
    if(rISP_CHG_CTL & 0x10)
    {
        DRV_SoftwareWakeup();
        //need delay 100ms(minimum) to wait ISP command, Don't remove this delay command
        DelayWhile(100); //This time MCU change source clock to IRC 12 MHz
        rISP_CHG_CTL = 0x00; //Disable ISP change clock. MCU go back to original setting
        rISP_CHG_CTL = 0xA0; //Enable ISP change clock
    }
}
```

Code Option setting General-purpose I/O Complex Function mapping registers, including Crystal Oscillator pins, Crystal oscillator Source option setting.

System Clock Source Control Register SOURCE_CLK_SLT (XFR: 0x05) **Reset Value: A1h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				SOURCE_CLK_SLT[1:0]		MCU_CLK_SLT[1:0]	

Bit Number	Bit Mnemonic	Description
7-4	-	Must be equal to “1010”, otherwise bit [3:0] cannot be written into.
3-2	SOURCE_CLK_SLT[1:0]	Select SOURCE clock sources 00: internal 12 MHz RC oscillator (default) 01: external DC ~ 16 MHz crystal oscillator 10: internal 32 kHz RC oscillator 11: reserved Default value can be selected by section 6.20 Code Option
1-0	MCU_CLK_SLT[1:0]	MCU clock setting 00: MCU clock and System clock = SOURCE clock (default) 01: MCU clock and System clock = SOURCE clock /2 10: MCU clock and System clock = SOURCE clock /4 11: MCU clock and System clock = SOURCE clock /12

-: unimplemented.

Notes:

1. When SOURCE clock selects internal 32 kHz RC oscillator and the system clock source of the Watch Timer selects External 32.768 kHz crystal oscillator, Interrupt sources cannot be captured in time due to Internal 32 kHz RC oscillator with huge tolerance and the execute speed is slower than the Interrupt generaed by Watch Timer. In this mode, it requires having the External Clock Source Prescaler Control Register 1 and External Clock Source Prescaler Control Register 2 setting divided by 2, and the Watch Timer clock source divided by 2 equals to 16.384 kHz. In the meantime, the time period selected by the Watch Timer will be extended twice to capture completely without missing.

Setting External Clock Source/ 2 procedures:

1. Setting Prescaler Data: CRY_DIV[9:0] = 1, and 32.768 kHz/(CRY_DIV[9:0]+1) = 32.768 kHz/2 =16.384 kHz
2. Enable external crystal oscillator clock source prescaler: EN_CRY_DIV = 1

Power-saving Control Register POWER_SAVE_CTL (XFR: 0x06) **Reset Value: 50h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				MCU_CLK_OFF	SYSTEM_CLK_OFF	SOURCE_CLK_OFF	IRC12M_CLK_OFF

Bit Number	Bit Mnemonic	Description
7-4	-	Must be equal to “0101”; otherwise, Bit[3:0] cannot be written into.
3	MCU_CLK_OFF	1: MCU clock is Off (including MCU and partial peripheral hardware), and MCU must wait for 3~4 MCU clock cycles until MCU clock ON and work. 0: MCU clock is On.

Bit Number	Bit Mnemonic	Description
2	SYSTEM_CLK_OFF	1: MCU clock is Off (including MCU and partial peripheral hardware), and MCU must wait for 3~4 MCU clock cycles until system clock ON and work. 0: MCU clock is On.
1	SOURCE_CLK_OFF (bias OFF)	1: SOURCE clock is Off. SOURCE clock sources: (MCU clock is turned off and bias OFF) External 12 MHz or 32.768 kHz crystal oscillator, and MCU must wait for 16*1024 SYSTEM clock cycles until source clock ON and work. Internal 12 MHz oscillator, and MCU must wait for 131~132 SYSTEM clock cycles until source clock ON and work. Internal 32 kHz RC oscillator, and MCU must wait for 8 SYSTEM clock cycles until source clock ON and work. 0: MCU clock is On.
0	IRC12M_CLK_OFF (bias ON)	1: Internal 12 MHz RC oscillator is Off and bias ON MCU must wait for 11~12 IRC12M clock cycles until IRC12M ON and work. 0: MCU clock is On.

-: unimplemented.

Note: Refer to section 3.1 System Clock Tree for more details.

Clock Source Control Register IRC_12M_PD (XFR: 0x07) **Reset Value: A2h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	R/W	R/W	R/W	R/W	-
Name	Reserved			IRC_12M_PD1	IRC_12M_PD2	IRC_32K_PD	CRY_12M_PD	Reserved

Bit Number	Bit Mnemonic	Description
7-5	-	Must be equal to “101”, otherwise bit[4:0] cannot be written into
4	IRC_12M_PD1	1: partial internal 12 MHz RC oscillator power is turned off (default value is not off) 0: not off Default value can be selected by section 6.20 Code Option
3	IRC_12M_PD2	1: all internal 12 MHz RC oscillator power is turned off (default value is not off) 0: not off Default value can be selected by section 6.20 Code Option
2	IRC_32K_PD	1: internal 32 kHz RC oscillator power is turned off (default value is not off) 0: not off Default value can be selected by section 6.20 Code Option
1	CRY_12M_PD	1: external 12 MHz ~ 32 kHz crystal oscillator power is turned off (default value is off) 0: not off Default value can be selected by section 6.20 Code Option
0	Reserved	-

-: unimplemented.

Oscillator Driver Control Register CRY_12M_DR[2:0] (XFR: 0x08) **Reset Value: 58h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				CRY_12M_DR[2:0]			SLT_CRYSTAL

Bit Number	Bit Mnemonic	Description
7-4	-	Must be equal to “0101”, otherwise, Bit[3:0] cannot be written into
3-1	CRY_12M_DR[2:0]	External oscillator driving ability setting 000: crystal oscillator with frequency of 32.768 kHz (VDD > 2.4V) 001: crystal oscillator with frequency of 32.768 kHz 010: crystal oscillator with frequency of 100 kHz 100: crystal oscillator with frequency of 1 MHz ~ 12 MHz (default) 110: crystal oscillator with frequency of 12 MHz ~ 16 MHz Default value can be selected by section 6.20 Code Option
0	SLT_CRYSTAL	Crystal Oscillator Input pin selection 1: the crystal oscillator input pins of path 2. **MOSCI2 (GPIOF0), MOSCO2 (GPIOF1)** 0: the crystal oscillator input pins of path 1. **MOSCI1 (GPIOA5), MOSCO1 (GPIOA4)** Default value can be selected by section 6.20 Code Option

-: unimplemented.

General-purpose I/O Port Wakeup Control Register 1 GPIO_WK[15:8] (XFR: 0x60) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIO_WK[15:8]							

Bit Number	Bit Mnemonic	Description
7-0	GPIO_WK[15:8]	General-purpose I/O Port Wakeup MCU Enable setting Bit 7 = 1: Enable General-purpose I/O Port A7 Wakeup MCU function; 0: function disabled Bit 6 = 1: Enable General-purpose I/O Port A6 Wakeup MCU function; 0: function disabled Bit 5 = 1: Enable General-purpose I/O Port A3 Wakeup MCU function; 0: function disabled Bit 4 = 1: Enable General-purpose I/O Port A2 Wakeup MCU function; 0: function disabled Bit 3 = 1: Enable General-purpose I/O Port A1 Wakeup MCU function; 0: function disabled Bit 2 = 1: Enable General-purpose I/O Port A0 Wakeup MCU function; 0: function disabled Bit 1 = 1: Enable General-purpose I/O Port B7 Wakeup MCU function; 0: function disabled Bit 0 = 1: Enable General-purpose I/O Port B5 Wakeup MCU function; 0: function disabled

General-purpose I/O Port Wakeup Control Register 2 GPIO_WK[7:0] (XFR: 0x61) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	GPIO_WK[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIO_WK[7:0]	General-purpose I/O Port Trigger Wakeup MCU Enable setting Bit 7 = 1: Enable General-purpose I/O Port B4 Trigger Wakeup MCU function; 0: function disabled Bit 6 = 1: Enable General-purpose I/O Port B3 Trigger Wakeup MCU function; 0: function disabled Bit 5 = 1: Enable General-purpose I/O Port B2 Trigger Wakeup MCU function; 0: function disabled Bit 4 = 1: Enable General-purpose I/O Port E7 Trigger Wakeup MCU function; 0: function disabled Bit 3 = 1: Enable General-purpose I/O Port E6 Trigger Wakeup MCU function; 0: function disabled Bit 2 = 1: Enable General-purpose I/O Port E3 Trigger Wakeup MCU function; 0: function disabled Bit 1 = 1: Enable General-purpose I/O Port E2 Trigger Wakeup MCU function; 0: function disabled Bit 0 = 1: Enable General-purpose I/O Port E0 Trigger Wakeup MCU function; 0: function disabled

Peripheral Interrupt Wakeup Control Register PERIPHERAL_WK (XFR: 0x64) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W		R/W	-
Name	INT_WK[3:0]				ADC_WK	Reserved	WTMR_WK	Reserved

Bit Number	Bit Mnemonic	Description
7-4	INT_WK[3:0]	External 8052 INT0/1/3 Wakeup MCU Enable setting Bit 7 = 1: Enable 8052 INT3 Wakeup MCU function; 0: function disabled Bit 6 = reserved Bit 5 = 1: Enable 8052 INT1 Wakeup MCU function; 0: function disabled Bit 4 = 1: Enable 8052 INT0 Wakeup MCU function; 0: function disabled
3	ADC_WK	ADC Wakeup MCU Enable setting 1: Enable Wakeup MCU function after ADC compare is complete 0: Disable Wakeup MCU function after ADC compare is complete
2	Reserved	-
1	WTMR_WK	Watch Timer Wakeup MCU Enable setting 1: Enable Watch Timer Wakeup MCU function after Watch Timer is triggered

Bit Number	Bit Mnemonic	Description
		0: Disable Watch Timer Wakeup MCU function after Watch Timer is triggered
0	Reserved	-

-: unimplemented.

General-purpose I/O Port Wakeup Flag Register 1 GPIO_TOG[15:8] (XFR: 0x65) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	GPIO_TOG[15:8]							

Bit Number	Bit Mnemonic	Description
7-0	GPIO_TOG[15:8]	General-purpose I/O Port Trigger Wakeup Flag. If the corresponding bit Toggle Trigger occurred, Wakeup Flag Bit = 1 Bit 7: I/O Port A7 Wakeup Flag Bit 6: I/O Port A6 Wakeup Flag Bit 5: I/O Port A3 Wakeup Flag Bit 4: I/O Port A2 Wakeup Flag Bit 3: I/O Port A1 Wakeup Flag Bit 2: I/O Port A0 Wakeup Flag Bit 1: I/O Port B7 Wakeup Flag Bit 0: I/O Port B5 Wakeup Flag

General-purpose I/O Port Wakeup Flag Register GPIO_TOG[7:0] (XFR: 0x66) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	GPIO_TOG[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	GPIO_TOG[7:0]	General-purpose I/O Port Trigger Wakeup Flag. If the corresponding bit Toggle Trigger occurred, Wakeup Flag Bit = 1 Bit 7: I/O Port B4 Wakeup Flag Bit 6: I/O Port B3 Wakeup Flag Bit 5: I/O Port B2 Wakeup Flag Bit 4: I/O Port E7 Wakeup Flag Bit 3: I/O Port E6 Wakeup Flag Bit 2: I/O Port E3 Wakeup Flag Bit 1: I/O Port E2 Wakeup Flag Bit 0: I/O Port E0 Wakeup Flag

Peripheral Interrupt Wakeup Flag Register PERIPHERAL_TOG (XFR: 0x69) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	-	R	-
Name	INT_WK_EVT[3:0]				ADC_TOG	Reserved	WTMR_EVT	Reserved

Bit Number	Bit Mnemonic	Description
7-4	INT_WK_EVT[3:0]	Interrupt Wakeup Flag

Bit Number	Bit Mnemonic	Description
		Bit 7 = 1: MCU has been woken up by INT3 interrupt Bit 6 = reserved Bit 5 = 1: MCU has been woken up by INT1 interrupt Bit 4 = 1: MCU has been woken up by INT0 interrupt
3	ADC_TOG	ADC Trigger (Wakeup) Flag 1: a Trigger (Wakeup) occurred in ADC 0: a Trigger (Wakeup) not occurred in ADC
2	Reserved	-
1	WTMR_EVT	Watch Timer Trigger (Wakeup) Flag 1: a Trigger (Wakeup) occurred in Watch Timer 0: a Trigger (Wakeup) not occurred in Watch Timer
0	Reserved	-

-: unimplemented.

Wakeup Clear Register CLR_IN_TOG (XFR: 0x6A) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	-	-	-	-	-	-	R
Name	CLR_IN_TOG	Reserved						IN_TOG

Bit Number	Bit Mnemonic	Description
7	CLR_IN_TOG	1: Clear all Input Toggle
6-1	Reserved	-
0	IN_TOG	1: All toggle events logic- or operation if any toggle source occurred, this bit will be set.

-: unimplemented.

The setting of entering Sleep Mode and Wakeup procedure:

1. Set RST_NDF = 1
2. Disable Watchdog Timer (DIS_WDT[7:5] = 101)
3. Select Wakeup sources:

		Idle 1	Idle 2	Sleep Mode
SOURCE		MCU_CLK_OFF	SYSTEM_CLK_OFF	SOURCE_CLK_OFF IRC12M_CLK_OFF
NRST		●	●	●
GPIOx_WK[x]		●	●	●
INT0/1_WK	IE0/1_ADC			
	IE0/1_WTMR			
	IE0/1_ETIMER	●		
	IE0/1_IN_TOG	●	●	●
INT3_WK	IRQ[7:0]	●		
ADC_WK		●	●	●
WTMR_WK		●	●	●

4. Clear all input Trigger Wakeup (CLR_IN_TOF = 1)
5. SOURCE clock select internal 12 MHz RC oscillator (SOURCE_CLK_SLT[1:0] = 00)
6. Entering Sleep Mode (SOURCE_CLK_OFF = 1)
7. Wait for Wakeup Trigger
   SOURCE clock = IRC 12M, needs to wait for 132 clock cycles to return to the main program
   SOURCE clock = Crystal, needs to wait for 16 x 1024 clock cycles to return to the main program

6.8 12 MHz RC Oscillator Calibration

WT56F116S/108S has a built-in 12/24 MHz RC oscillator to reduce the cost of external crystal oscillator. For more precise system clock, external crystal oscillator 12/24 MHz is available. In addition, it is a better choice to use 32.768 kHz (crystal oscillator) to calibrate internal RC 12/24 MHz oscillators. (Calibration can reach ±2% at -40℃ ~ +105℃)

Internal Oscillator Adjust Register RC_LADJ (XFR: 0x70) **Reset Value: 40h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved	RC_LADJ[6:0]						

Bit Number	Bit Mnemonic	Description
7	Reserved	-
6-0	RC_LADJ[6:0]	Each level 0.5% fine adjustment of the Internal RC oscillator frequency (default value ‘40H’), 127 levels in total

-: unimplemented.

Note: Internal Oscillator Adjustment Register RC_LADJ[6:0] is allowed to adjust the control circuit of IRC 12/24 MHz directly.

Internal Oscillator Counter Data High Bytes Register RC12M_CNT[9:2] (XFR: 0x71) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	RC12M_CNT[9:2]							

Bit Number	Bit Mnemonic	Description
7-0	RC12M_CNT[9:2]	The counting value RC12M_CNT[9:2] of internal 12/24 MHz RC oscillator, is paired with RC12M_CNT[1:0] to form a 10-bit counting value

Internal Oscillator Counter Data Low Bytes Register RC12M_CNT[1:0] (XFR: 0x72) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	-	R	R
Name	Reserved						RC12M_CNT[1:0]	

Bit Number	Bit Mnemonic	Description
7-2	Reserved	-
1-0	RC12M_CNT[1:0]	The counting value RC12M_CNT[1:0] of internal 12/24 MHz RC oscillator, is paired with RC12M_CNT[9:2] to form a 10-bit counting value

-: unimplemented.

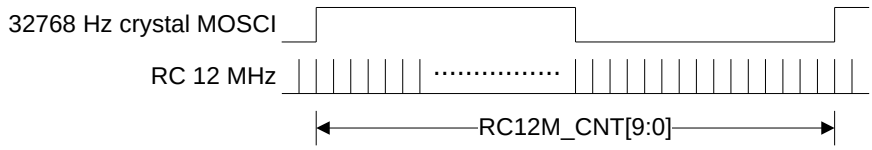
Internal Oscillator Calibration Control Register RC_CALIB_EN (XFR: 0x73) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	-	R/W	-	-	-	-	-
Name	RC_CALIB_EN	Reserved	AUTO_CAL_EN	Reserved				

Bit Number	Bit Mnemonic	Description
7	RC_CALIB_EN	1: Enable RC Oscillator Calibration function
6	Reserved	-
5	AUTO_CAL_EN	1: Enable H/W automatic calibration function
4-0	Reserved	-

-: unimplemented.

Note:
Manual calibration: enable RC_CALIB_EN, and is working together with Firmware.
Automatic calibration: enable RC_CALIB_EN and AUTO_CAL_EN.



Calibration Theory:

When the external 32.768 kHz oscillator is used, it is available to count in the fixed width of precise 32.768 kHz by internal RC 12 MHz. Then with the counting value we got, we can make a compensation by controlling the Internal Oscillator Adjust Registers RC_LADJ[6:0], reaching ±1% at room temperature.

The range of adjustment:

Coarse adjustment: the actual internal RC frequency ± (internal RC frequency * 0.08); RC_LADJ_C[2:0] ranges from 000 ~ 111, and the middle value is 100.

Fine adjustment: the actual internal RC frequency ± (internal RC frequency * 0.005); RC_LADJ_F[3:0] ranges from 0000 ~ 1111, and the middle value is 1000.

RC 12MHz

RC12M_CNT[9:0]	External 32.768 kHz Sampled (Hz)	Target Value (Hz)	Tolerance %
360	11796480	12000000	+1.70
361	11829248	12000000	+1.42
362	11862016	12000000	+1.15
363	11894784	12000000	+0.88
364	11927552	12000000	+0.60
365	11960320	12000000	+0.33
366	11993088	12000000	+0.06
367	12025856	12000000	-0.22

RC12M_CNT[9:0]	External 32.768 kHz Sampled (Hz)	Target Value (Hz)	Tolerance %
368	12058624	12000000	-0.49
369	12091392	12000000	-0.76
370	12124160	12000000	-1.03

RC 24MHz

RC12M_CNT[9:0]	External 32.768 kHz Sampled (Hz)	Target Value (Hz)	Tolerance %
727	23822336	24000000	-0.74
728	23855104	24000000	-0.6
729	23887872	24000000	-0.47
730	23920640	24000000	-0.33
731	23953408	24000000	-0.19
732	23986176	24000000	-0.06
733	24018944	24000000	+0.08
734	24051712	24000000	+0.22
735	24084480	24000000	0.35
736	24117248	24000000	0.49
737	24150016	24000000	0.63

Notes:

1. When WT56F116S/108S has been woken up from Sleep mode (RC bias is turned on), RC oscillator calibration function needs to wait for at least 83.3ns (at 12 MHz) to return to normal mode.
2. As soon as the RC oscillator calibration function is enabled, read RC12M_CNT[9:2] & RC12M_CNT[1:0] registers twice, then confirm the data is the same to proceed with the calibration process.
3. If RC12M_CNT[9:0] Internal Oscillator Counter Data Register is 1023 (0x3FF), indicating that no external oscillator or without enabling external oscillator.
4. When reset, WT56F116S/108S will auto-reload the calibration value of RC 12 MHz into Internal Oscillator Adjustment Register (XFR: 0x70).
   To switch to RC 24MHz, HFIRC_CLK_SLT (XFR_0x01_bit2) must be set by program and load the corresponding calibration value.
   IRC Oscillator (12/24M) switching procedures:
   (a) IRC12M change to IRC24M
      (1) Set HFIRC_CLK_SLT
      (2) Move flash memory XDATA 0x0E07H-bit[6:0] to XFR_0x70 register
   (b) IRC24M change to IRC12M
      (1) Clear HFIRC_CLK_SLT
      (2) Move flash memory XDATA 0x0E03H-bit[6:0] to XFR_0x70 register
5. When enable AUTO_CAL_EN & the external 32.768 kHz oscillator of MCU is also oscillated, MCU will auto calibrate once every 30.5us.
   (condition: CRY_12M_PD, IRC_12M_PD1 & IRC_12M_PD2 cannot be turned off).

6.9 Watchdog Timer and Watch Timer

6.9.1 Watchdog Timer (WDT)

Watchdog Timer can be used to detect CPU failures, such as the software deadlock circles caused by noises, voltage disturbance, or power off etc. When an internal counter of the Watchdog Timer overflows, a reset signal will be generated then reset the CPU.

Watchdog Timer is not similar to the general-purpose 8052 Timer 0/1. To prevent a reset occurred on Watchdog Timer, which can be cleared by software before important path of program. When unpredictable reset occurred, user should check the WDT_RST_FLG bit in Reset Flag Register to judge if the previous reset is occurred by Watchdog Timer.

- Clock sources of Watchdog Timer: Internal 32 kHz, or External 32.768 kHz Crystal Oscillator
- Reset Time: 16 ms, 32 ms, 1.024 S or 2.048 S

Watchdog Timer Control Register WDT_CTL (XFR: 0x78) **Reset Value: 02h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	-	-	-	R/W	R/W
Name	DIS_WDT[2:0]			Reserved			WDT_TM_SLT[1:0]	

Bit Number	Bit Mnemonic	Description
7-5	DIS_WDT[2:0]	Watchdog Timer switch 101: Disable Watchdog Timer at the same time clear counts Other value: Enable Watchdog Timer, and also based on the setting of WDT_TM_SLT[1:0] to reset Watchdog Timer Counter
4-2	Reserved	-
1-0	WDT_TM_SLT[1:0]	Watchdog Reset Time setting When the Watchdog uses internal RC 32 kHz oscillator: 00: 16 ms 01: 32 ms 10: 1.024 S 11: 2.048 S When the Watchdog uses external 32.768 kHz Crystal Oscillator: 00: 15.625 ms 01: 31.25 ms 10: 1 S 11: 2 S

-: unimplemented.

Notes:

1. The frequency tolerance of internal 32 kHz RC oscillator is about ±30%.
2. The Watchdog Timer clock sources can by selected by the bit WDT_CLK_SLT of System Control Register (XFR: 0x01), with details as below.

System Control Register SYS_CTL (XFR: 0x01) **Reset Value: 80h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	-	-	-	R/W	R/W
Name	RST_NDF	LVD_RST_LVL_ADJ	EN_PC_OVL_RST	CRY_CLK_	RST_NDF	LVD_RST_LVL_ADJ	EN_PC_OVL_RST	CRY_CLK_

Bit Number	Bit Mnemonic	Description
7	RST_NDF	1: NRST pin without digital filter function 0: NRST pin with digital filter function (4 clocks)
6	LVD_RST_LVL_ADJ	1: +0.25V 0: +0V
5	EN_PC_OVL_RST	1: Enable program counter overflow reset 0: Disable program counter overflow reset
4	CRY_CLK_DIV2	1: Enable “External Crystal Oscillator Prescaler” /2
3	BGP_VOL_SLT	1: bandgap = 2.44V 0: bandgap = 1.23V
2	HFIRC_CLK_SLT	1: Internal IRC oscillator = 24 MHz 0: Internal IRC oscillator = 12 MHz
1	WDT_CLK_SLT	1: Watchdog Timer uses external 12 MHz ~ 32.768 kHz crystal oscillator 0: Watchdog Timer uses internal 32 kHz RC oscillator
0	WTMR_CLK_SLT	1: Watch Timer uses external 12 MHz ~ 32.768 kHz crystal oscillator 0: Watch Timer uses internal 32 kHz RC oscillator

-: unimplemented.

Note: If WDT_CLK_SLT = 1 or WTMR_CLK_SLT = 1, must enable EN_CRY_DIV simultaneously and set CRY_DIV[9:0] to allow Watchdog Timer use precise clock source 32 kHz. If External Crystal Oscillator = 32.768 kHz, then it is no need to enable EN_CRY_DIV.

External Clock Source Prescaler Control Register 1 CRY_DIV[9:8] (XFR: 0x09) **Reset Value: 01h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	-	-	-	-	-	R/W	R/W
Name	EN_CRY_DIV	Reserved					CRY_DIV[9:8]	

Bit Number	Bit Mnemonic	Description
7	EN_CRY_DIV	1: Enable clock source prescaler of external crystal oscillator 0: Disable clock source prescaler of external crystal oscillator
6-2	Reserved	-
1-0	CRY_DIV[9:8]	The prescaler data [9:8] of external Crystal oscillator clock source, is paired with CRY_DIV[7:0] to form a 10-bit prescaler data

-: unimplemented.

External Clock Source Prescaler Control Register 2 CRY_DIV[7:0] (XFR: 0x0A) **Reset Value: 76h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	CRY_DIV[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	CRY_DIV[7:0]	The prescaler data [7:0] of external Crystal oscillator clock source, is paired with CRY_DIV[9:8] to form a 10-bit prescaler data

Note: When enable EN_CRY_DIV, CRY_DIV[9:0] cannot be set as 0, or MCU cannot work normally.

Examples:

1. If the clock source is External 24 MHz crystal oscillator, and the Watchdog Timer and Watch Timer use the clock source with low tolerance frequency (for precise time base), then the External Clock Source Prescaler Control Register must be enabled and the prescaler data is required.
    1. Setting prescaler data: CRY_DIV[9:0] = 731; 24 MHz / (CRY_DIV[9:0] + 1) = 24 MHz/732 = 32.768 kHz
    2. Enable clock source prescaler of external crystal oscillator: EN_CRY_DIV = 1
    3. Select the clock source of Watchdog Timer & Watch Timer as External Oscillator: WDT_CLK_SLT = 1; WTMR_CLK_SLT = 1
2. If the clock source is External 12 MHz crystal oscillator, and the Watchdog Timer and Watch Timer use the clock source with low tolerance frequency (for precise time base), then the External Clock Source Prescaler Control Register must be enabled and the prescaler data is required.
    1. Setting prescaler data: CRY_DIV[9:0] = 365; 12 MHz / (CRY_DIV[9:0] + 1) = 12 MHz/366 = 32.768 kHz
    2. Enable clock source prescaler of external crystal oscillator: EN_CRY_DIV = 1
    3. Select the clock source of Watchdog Timer & Watch Timer as External Oscillator: WDT_CLK_SLT = 1; WTMR_CLK_SLT = 1
3. If the clock source is Internal 32 kHz crystal oscillator, and the Watchdog Timer and Watch Timer use the clock source with external 32.768 kHz, then the External Clock Source Prescaler Control Register must be enabled and the prescaler data is required.
    1. Setting prescaler data: CRY_DIV[9:0] =0; 32.768 kHz/(CRY_DIV[9:0] + 1) = 32.768 kHz/2 = 16.384 kHz
    2. Enable clock source prescaler of external crystal oscillator: EN_CRY_DIV = 1
    3. Select the clock source of Watchdog Timer & Watch Timer as External Oscillator: WDT_CLK_SLT = 1; WTMR_CLK_SLT = 1

6.9.2 Watch Timer

The application functions of Watch Timer include Timer Interrupt, Timer Wakeup, LCD display frequency and so on.

- The clock source of Watch Timer is 32 kHz internal RC oscillator or 32.768 kHz external oscillator. By this clock, it can generate eight Time bases
- Watch Timer can also be served as the display frequency sources of LCD Driver, with five frequencies to select. (Refer to LCD Driver section)

Watch Timer Control Register WTMR_CTL (XFR: 0x7C) **Reset Value: 80h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R	W	-	-	-	-	-
Name	DIS_WTMR	WTMR_EVT	CLR_WTMR_EVT	Reserved				

Bit Number	Bit Mnemonic	Description
7	DIS_WTMR	1: Disable Watch Timer 0: Enable Watch Timer
6	WTMR_EVT	1: Indicates Watch Timer Event (the setting time of Watch Timer as the count reaches WTMR_SLT[2:0]) 0: Cleared by CLR_WTMR_EVT = 1
5	CLR_WTMR_EVT	1: Clear Watch Timer event, and then WTMR_EVT = 0
4-0	Reserved	-

-: unimplemented.

Watch Timer Output Selection Register WTMR_SLT[2:0] (XFR: 0x7D) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	R/W	R/W	R/W
Name	Reserved					WTMR_SLT[2:0]		

Bit Number	Bit Mnemonic	Description
7-3	Reserved	-
2-0	WTMR_SLT[2:0]	Watch Timer Time base selection bit (If needs to be precise, using external Crystal Oscillator 32.768 kHz) is recommended. 000: watch time = 3.91 ms 001: watch time = 31.25 ms 010: watch time = 62.50 ms 011: watch time = 125 ms 100: watch time = 0.25 S 101: watch time = 0.5 S 110: watch time = 1 S 111: watch time = 2 S

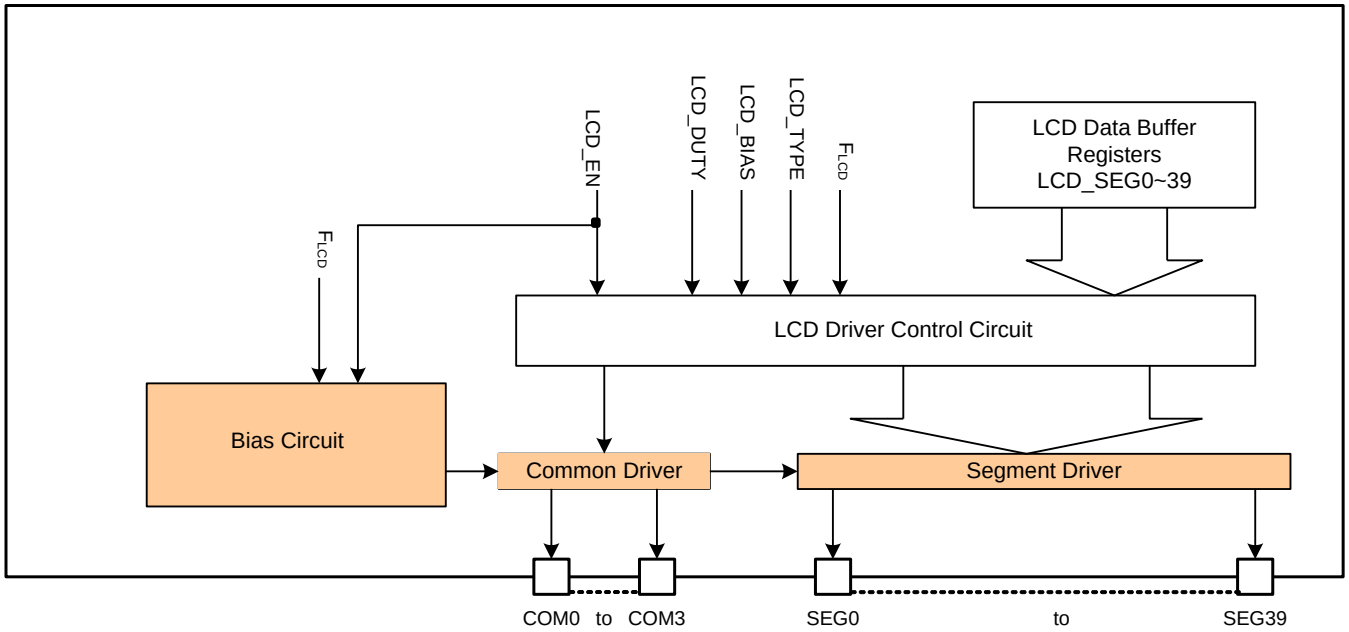
-: unimplemented.

6.10 LCD Driver

WT56F116S/108S contains LCD driver and control Circuit to drive LCD panel directly. Internal RC 32 kHz or external 32.768 kHz oscillator is available for LCD system clock source selection.

WT56F116S/108S supports LCD driver with below features:

- Built-in LCD Bias Voltages circuit with three selectable bias: 1/2 or 1/3 Bias
- Internal Register supports Duty Cycles adjustment: 1/2, 1/3, or 1/4 Duty
- Duty cycle/Bias/Frequency can be set by software
- When enabling LCD function, configure the Segment and the COM corresponding GPIO as Input.
- The display frequency source of LCD Driver is Watch Timer, please refer to 6.9.2 Watch Timer



LCD Driver Control Register 1 LCD_CTL1 (XFR: 0xA8) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	-	-	-	-	-	-
Name	LCD_EN	LCD_TYPE	Reserved					

Bit Number	Bit Mnemonic	Description
7	LCD_EN	LCD Power Control (During setting the related register of the LCD Driver, turning off the LCD power is essential.) 1: turn on LCD Driver power 0: turn off LCD Driver power
6	LCD_TYPE	LCD Driving waveform selection 1: B type driving waveform 0: A type driving waveform
5-0	Reserved	-

-: unimplemented.

LCD Driver Control Register 2 LCD_CTL2 (XFR: 0xA9) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	-	-
Name	LCD_CLK[2:0]			LCD_BIAS	LCD_DUTY[1:0]		Reserved	

Bit Number	Bit Mnemonic	Description
7-5	LCD_CLK[2:0]	LCD Scanned Frequency setting. If external 32.768 kHz oscillator is selected as LCD system clock source, scanned frequency is 2048 Hz when set LCD_CLK[2:0] = 000 (please refer to "LCD Driver Frame frequency setting table" for more details). 000 = $fs/2^4$ (if fs = 32.768 kHz, lcd_clk = 2048 Hz) 001 = $fs/2^5$ 010 = $fs/2^6$ 011 = $fs/2^7$ 1xx = $fs/2^8$
4	LCD_BIAS	LCD bias selection 1: 1/3 0: 1/2
3-2	LCD_DUTY[1:0]	LCD duty selection 00: static (1/2 duty and bias = VLCD) 01: 1/3 duty 1x: 1/4 duty
1-0	Reserved	-

-: unimplemented.

LCD Driver Segment Output Enable Register 1 LCD_SEG_EN[7:0] (XFR: 0xAB) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	LCD_SEG_EN[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	LCD_SEG_EN[7:0]	SEGDx output enable setting; 1: SEGDx output 0000_0001: enable SEGD0 data output 0000_0011: enable SEGD1~0 data output | 0111_1111: enable SEGD6~0 data output 1111_1111: enable SEGD7~0 data output

LCD Driver Segment Output Enable Register 2 LCD_SEG_EN[15:8] (XFR: 0xAC) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	LCD_SEG_EN[15:8]							

Bit Number	Bit Mnemonic	Description
7-0	LCD_SEG_EN[15:8]	SEGDx output enable setting; 1: SEGDx output 0000_0001: enable SEGD8 data output

Bit Number	Bit Mnemonic	Description
		0000_0011: enable SEGD9~8 data output | 0111_1111: enable SEGD14~8 data output 1111_1111: enable SEGD15~8 data output

LCD Driver Segment Output Enable Register 3 LCD_SEG_EN[23:16] (XFR: 0xAD) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	LCD_SEG_EN[23:16]							

Bit Number	Bit Mnemonic	Description
7-0	LCD_SEG_EN[23:16]	SEGDx output enable setting; 1: SEGDx output 0000_0001: enable SEGD16 data output 0000_0011: enable SEGD17~16 data output | 0111_1111: enable SEGD22~16 data output 1111_1111: enable SEGD23~16 data output

LCD Driver Segment Output Enable Register 4 LCD_SEG_EN[31:24] (XFR: 0xAE) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	LCD_SEG_EN[31:24]							

Bit Number	Bit Mnemonic	Description
7-0	LCD_SEG_EN[31:24]	SEGDx output enable setting; 1: SEGDx output 0000_0001: enable SEGD24 data output 0000_0011: enable SEGD25~24 data output | 0111_1111: enable SEGD30~24 data output 1111_1111: enable SEGD31~24 data output

Note: If the GPIO multiplexed with SEG did not use SEG, which allows LCD SEG mapping output pins as Tri-state by this Enable Register LCD_SEG_EN[31:0]

LCD Driver Display Data Register 0~39 LCD_SEGDx[7:0] (XFR: 0x80 ~ 0xA7) **Reset Value: 00h**

The table below is LCD display data Register mapping table:

4 COM LCD (COM0~3, SEG0~39)

Address	Register Name	7	6	5	4	3	2	1	0
						COM3	COM2	COM1	COM0
$80H	LCD_SEGD0[3:0]					SEG0	SEG0	SEG0	SEG0
$81H	LCD_SEGD1[3:0]					SEG1	SEG1	SEG1	SEG1
$82H	LCD_SEGD2[3:0]					SEG2	SEG2	SEG2	SEG2
$83H	LCD_SEGD3[3:0]					SEG3	SEG3	SEG3	SEG3
$84H	LCD_SEGD4[3:0]					SEG4	SEG4	SEG4	SEG4
$85H	LCD_SEGD5[3:0]					SEG5	SEG5	SEG5	SEG5
$86H	LCD_SEGD6[3:0]					SEG6	SEG6	SEG6	SEG6
$87H	LCD_SEGD7[3:0]					SEG7	SEG7	SEG7	SEG7
$88H	LCD_SEGD8[3:0]					SEG8	SEG8	SEG8	SEG8
$89H	LCD_SEGD9[3:0]					SEG9	SEG9	SEG9	SEG9
$8AH	LCD_SEGD10[3:0]					SEG10	SEG10	SEG10	SEG10
$8BH	LCD_SEGD11[3:0]					SEG11	SEG11	SEG11	SEG11
$8CH	LCD_SEGD12[3:0]					SEG12	SEG12	SEG12	SEG12
$8DH	LCD_SEGD13[3:0]					SEG13	SEG13	SEG13	SEG13
$8EH	LCD_SEGD14[3:0]					SEG14	SEG14	SEG14	SEG14
$8FH	LCD_SEGD15[3:0]					SEG15	SEG15	SEG15	SEG15
$90H	LCD_SEGD16[3:0]					SEG16	SEG16	SEG16	SEG16
$91H	LCD_SEGD17[3:0]					SEG17	SEG17	SEG17	SEG17
$92H	LCD_SEGD18[3:0]					SEG18	SEG18	SEG18	SEG18
$93H	LCD_SEGD19[3:0]					SEG19	SEG19	SEG19	SEG19
$94H	LCD_SEGD20[3:0]					SEG20	SEG20	SEG20	SEG20
$95H	LCD_SEGD21[3:0]					SEG21	SEG21	SEG21	SEG21
$96H	LCD_SEGD22[3:0]					SEG22	SEG22	SEG22	SEG22
$97H	LCD_SEGD23[3:0]					SEG23	SEG23	SEG23	SEG23
$98H	LCD_SEGD24[3:0]					SEG24	SEG24	SEG24	SEG24
$99H	LCD_SEGD25[3:0]					SEG25	SEG25	SEG25	SEG25
$9AH	LCD_SEGD26[3:0]					SEG26	SEG26	SEG26	SEG26
$9BH	LCD_SEGD27[3:0]					SEG27	SEG27	SEG27	SEG27
$9CH	LCD_SEGD28[3:0]					SEG28	SEG28	SEG28	SEG28
$9DH	LCD_SEGD29[3:0]					SEG29	SEG29	SEG29	SEG29
$9EH	LCD_SEGD30[3:0]					SEG30	SEG30	SEG30	SEG30
$9FH	LCD_SEGD31[3:0]					SEG31	SEG31	SEG31	SEG31

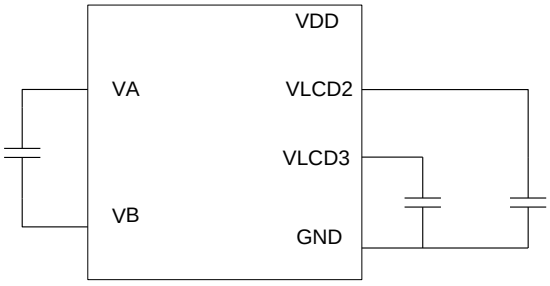
LCD Driver Bias table:

LCD Power Supply	1/2	1/3
V_{LCD} = VDD	V_{LCD}	V_{LCD}
VLCD2	-	2/3 V_{LCD}
VLCD3	1/2 V_{LCD}	1/3 V_{LCD}
VSS	VSS	VSS

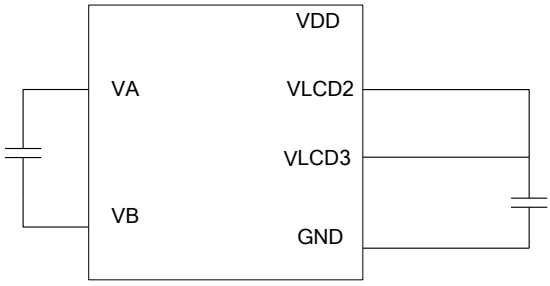
LCD Driver Frame frequency setting table:

LCD_Frame (LCD_CLK[2:0])	LCD_CLK (Hz)	Frame Frequency (Hz)		
	Clock	Static (1/2 Duty)	1/3 Duty	1/4 Duty
000	2048	1024	683	512
001	1024	512	341	256
010	512	256	171	128
011	256	128	85	64
1xx	128	64	43	32

Boost circuits connection for LCD voltage

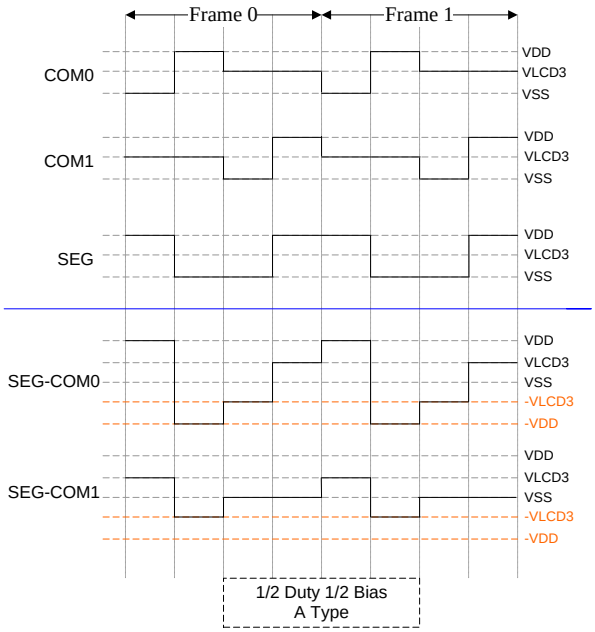


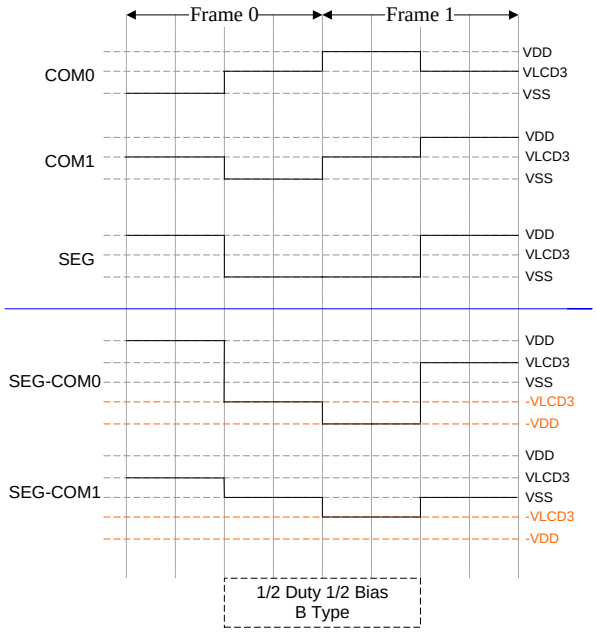
1/3 Bias peripheral circuit (C = 0.1uF)



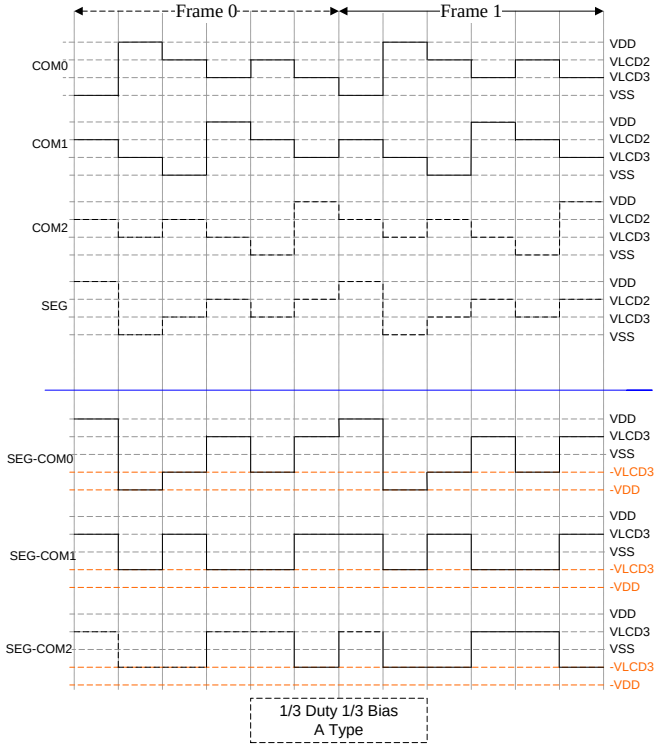
1/2 Bias peripheral circuit (C = 0.1uF)

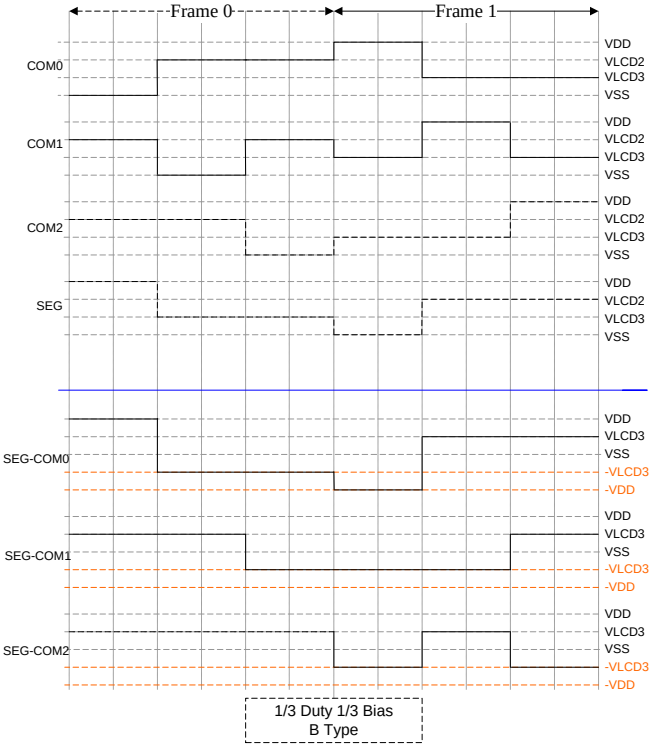
1/2 Duty, 1/2 Bias LCD driving waveform

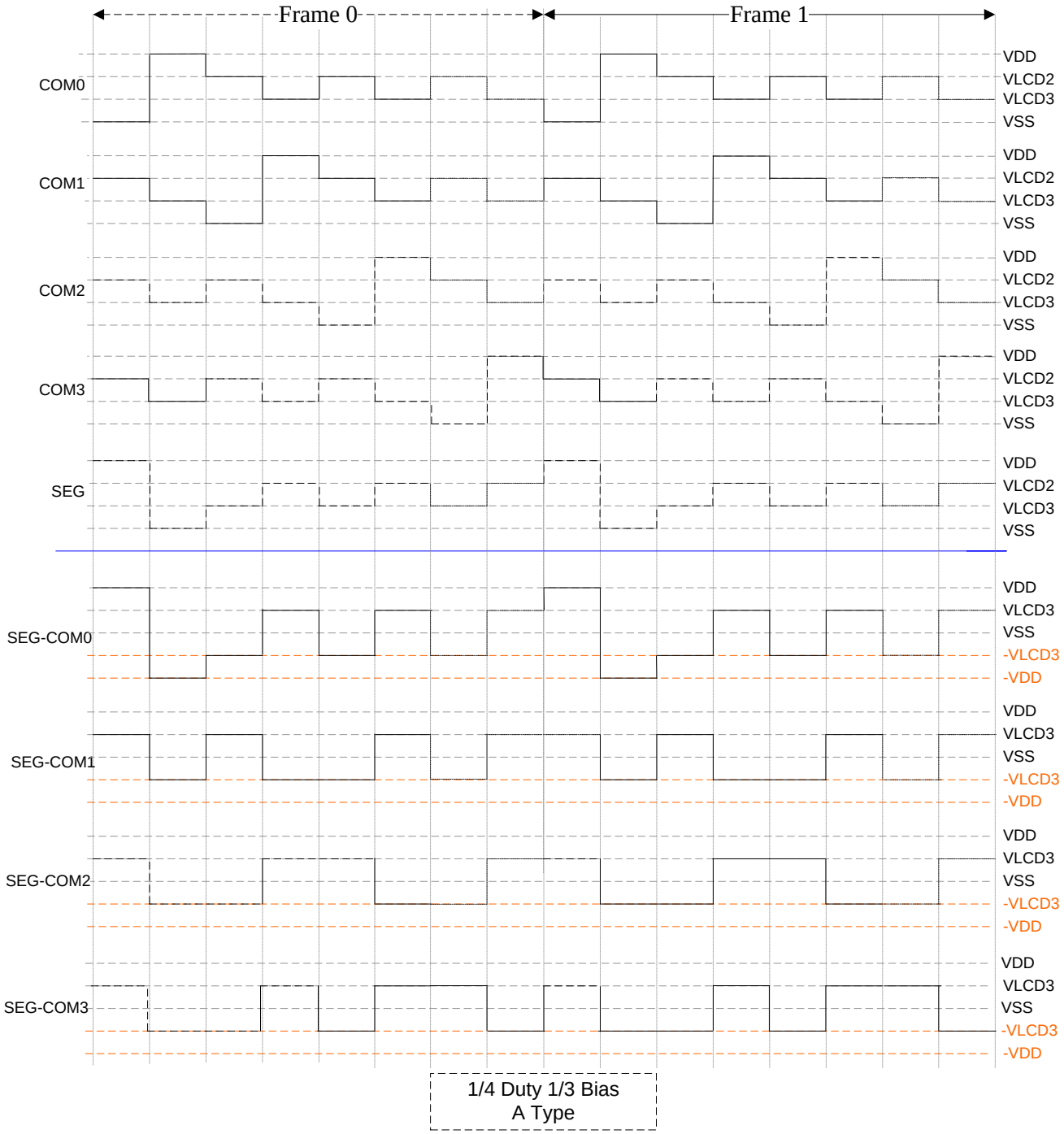




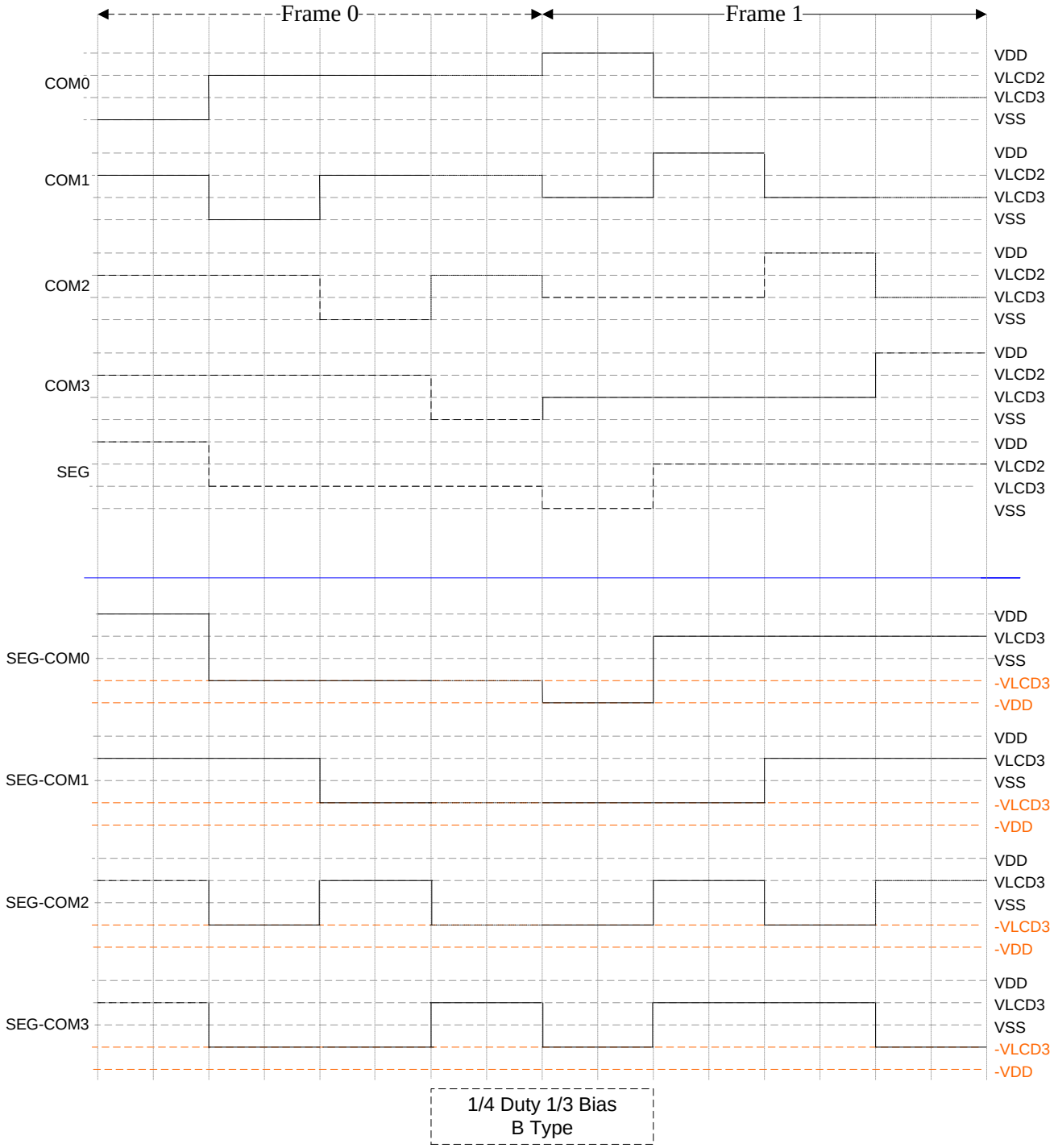
1/3 Duty, 1/3 Bias LCD driving waveform







1/4 Duty 1/3 Bias
A Type



6.11 I²C Serial Interface

I²C module uses SCL (clock) and SDA (data) wires to connect with other I²C interfaces. the transmission is determined by the software programmed MI²C_CLK [1:0] in XFR, and is allowed to reach 400 KBps (maximum). I²C module also provides Master/Slave mode, and it is set by Register.

Master/Slave I²C 0th Control Register MI²C_CTL0 (XFR: 0xB8) **Reset Value: 40h**

Master/Slave I²C 1st Control Register MI²C_CTL1 (XFR: 0xC8) **Reset Value: 40h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	W	W	R/W	W	W
Name	MI²C_EN	MI²C_CLK[1:0]		MI²C_START	MI²C_STOP	MI²C_TXNAK	MI²C_CLR_RT	MI²C_CLR_STP

Bit Number	Bit Mnemonic	Description
7	MI²C_EN	1: Enable I²C function 0: Disable I²C function
6-5	MI²C_CLK[1:0]	Select Master I²C Clock 00: SCL clock = 400 kHz at 12 MHz oscillator 01: SCL clock = 200 kHz at 12 MHz oscillator 10: SCL clock = 100 kHz at 12 MHz oscillator 11: SCL clock = 50 kHz at 12 MHz oscillator
4	MI²C_START	1: Enable I²C Transmit Start bit 0: Disable I²C Transmit Start bit
3	MI²C_STOP	1: Enable I²C Transmit Stop bit 0: Disable I²C Transmit Stop bit
2	MI²C_TXNAK	I²C Transmit ACK bit after next Rx state Bit 1: Transmit NACK Bit 0: Transmit ACK
1	MI²C_CLR_RT	1: Clear Transmit and Receive interrupt
0	MI²C_CLR_STP	1: Clear Slave mode Stop status interrupt

Master/Slave I²C 0th Status Register MI²C_STA0 (XFR: 0XB9) **Reset Value: 00h**

Master/Slave I²C 1st Status Register MI²C_STA1 (XFR: 0xC9) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	-
Name	MI²C_RDY	MI²C_INT_RT	MI²C_INT_STOP	MI²C_BB	MI²C_FIRST	MI²C_RW	MI²C_RXNAK	Reserved

Bit Number	Bit Mnemonic	Description
7	MI²C_RDY	When bit = 1, Interrupt status when I²C Receive/Transmit the 9th bit or Slave Stop phase
6	MI²C_INT_RT	When bit = 1, Interrupt status when I²C Receive/Transmit the 9th bit
5	MI²C_INT_STOP	When bit = 1, Interrupt status when I²C Slave mode Stop phase
4	MI²C_BB	When bit = 1, Slave mode bus busy
3	MI²C_FIRST	Slave mode First phase. This is the first byte from Master I²C with specific Slave Address.

Bit Number	Bit Mnemonic	Description
2	MI²C_RW	When bit = 1, Slave mode Read/Write Phase (the 8th bit of the first byte) 1: Slave I²C as Transmit mode 0: Slave I²C as Receive mode
1	MI²C_RXNAK	ACK bit indicator when I²C in Slave Tx mode 1: Master mode return NACK 0: Master mode return ACK
0	Reserved	-

-: unimplemented.

Master/Slave I²C 0th Transmit Buffer Register MI²C_DSLV0[7:0] (XFR: 0xBA) **Reset Value: 00h**

Master/Slave I²C 1st Transmit Buffer Register MI²C_DSLV1[7:0] (XFR: 0xCA) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	MI²C_DSLV[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	MI²C_DSLV[7:0]	Transmit slave address in Master mode

Master/Slave I²C 0th Transmit and Receive Buffer Register MI²C_DTRX0[7:0] (XFR: 0XBB)

Reset Value: FFh

Master/Slave I²C 1st Transmit and Receive Buffer Register MI²C_DTRX1[7:0] (XFR: 0XCB)

Reset Value: FFh

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	MI²C_DTRX[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	MI²C_DTRX[7:0]	I²C transmit and receive buffer W: When Tx work as I²C transmit buffer R: When Rx work as I²C receive buffer

Slave I²C 0th Address Register MI²C_SADR0 (XFR: 0xBC) **Reset Value: 00h**

Slave I²C 1st Address Register MI²C_SADR1 (XFR: 0xCC) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	MI²C_SADR							MI²C_SLVE

Bit Number	Bit Mnemonic	Description
7-1	MI²C_SADR	The slave address
0	MI²C_SLVE	I²C slave mode enable 1: I²C as Slave 0: I²C as Master

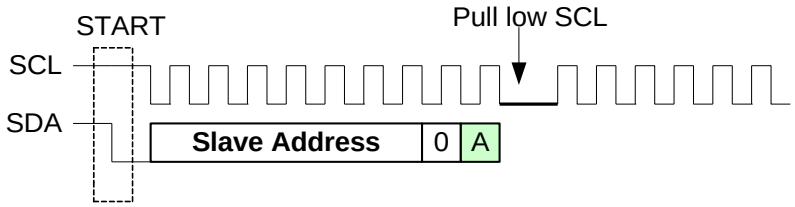
Master/Slave I²C 0th Extend Control Register MI²C_EXTEND0[7:0] (XFR: 0xBD) Reset Value: 00h
Master/Slave I²C 1st Extend Control Register MI²C_EXTEND1[7:0] (XFR: 0xCD) Reset Value: 00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	-	R/W	R/W
Name	Reserved						MI²C_AUTOSTP	MI²C_WAIT

Bit Number	Bit Mnemonic	Description
7-2	Reserved	-
1	MI²C_AUTOSTP	Enable Master I²C auto transmit stop bit, when receive NACK Bit
0	MI²C_WAIT	Enable Master/Slave I²C pull SCL low after the 9th bit

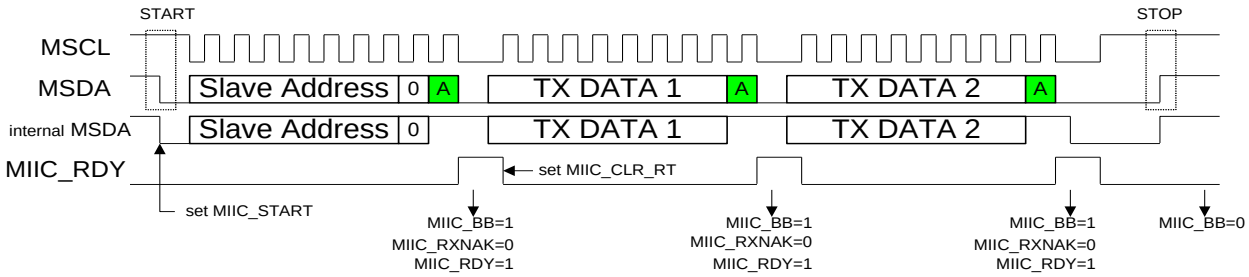
-: unimplemented.

If the firmware processing time is slower than the time of I²C receiving 9 bits, then the firmware must set MI²C_WAIT enabling WT51F116S/108S to pull SCL low after the 9th bit.

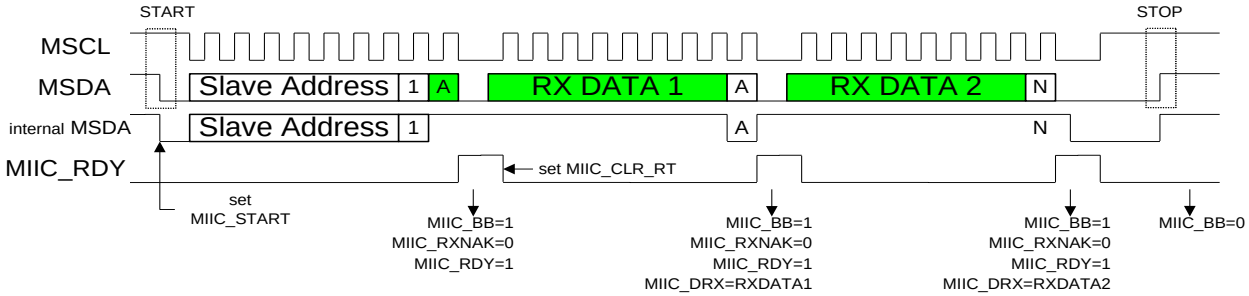


WT56F116S/108S Master/Slave I²C Data Flow

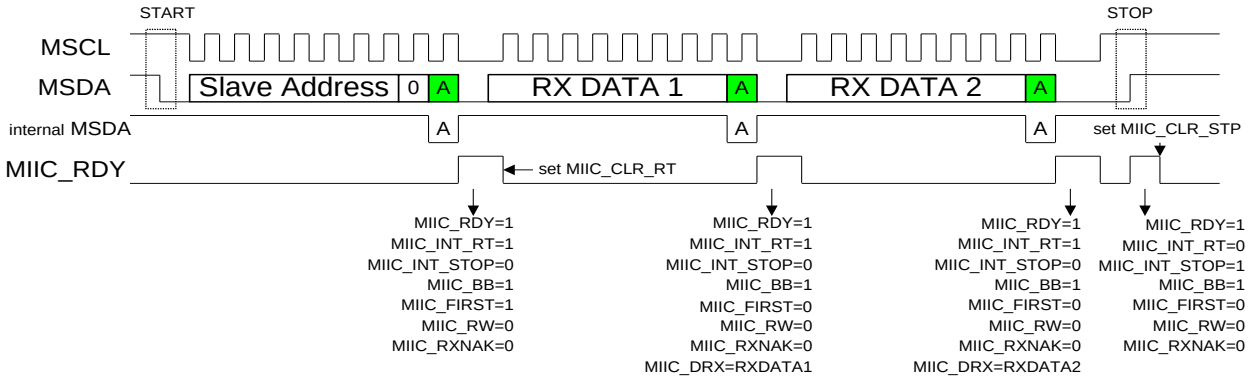
(1) Master write mode :



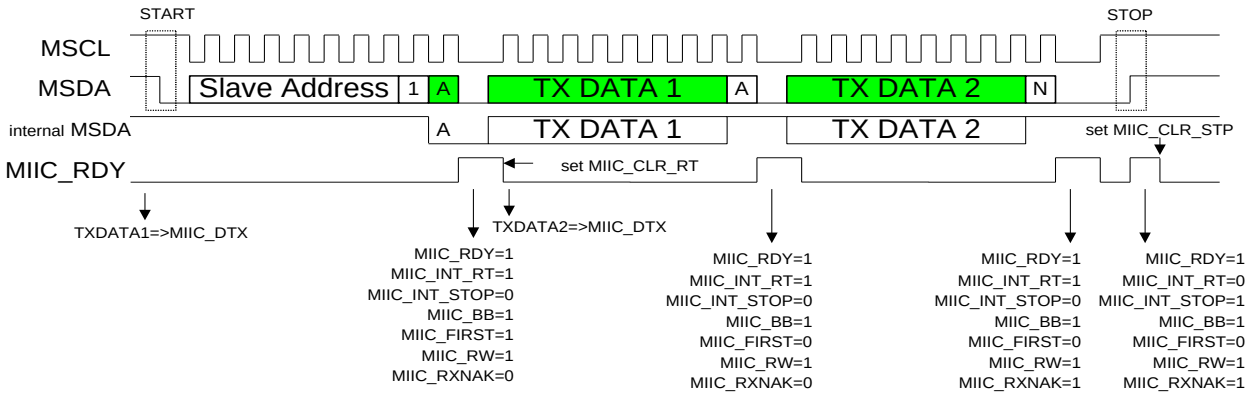
(2) Master read mode :



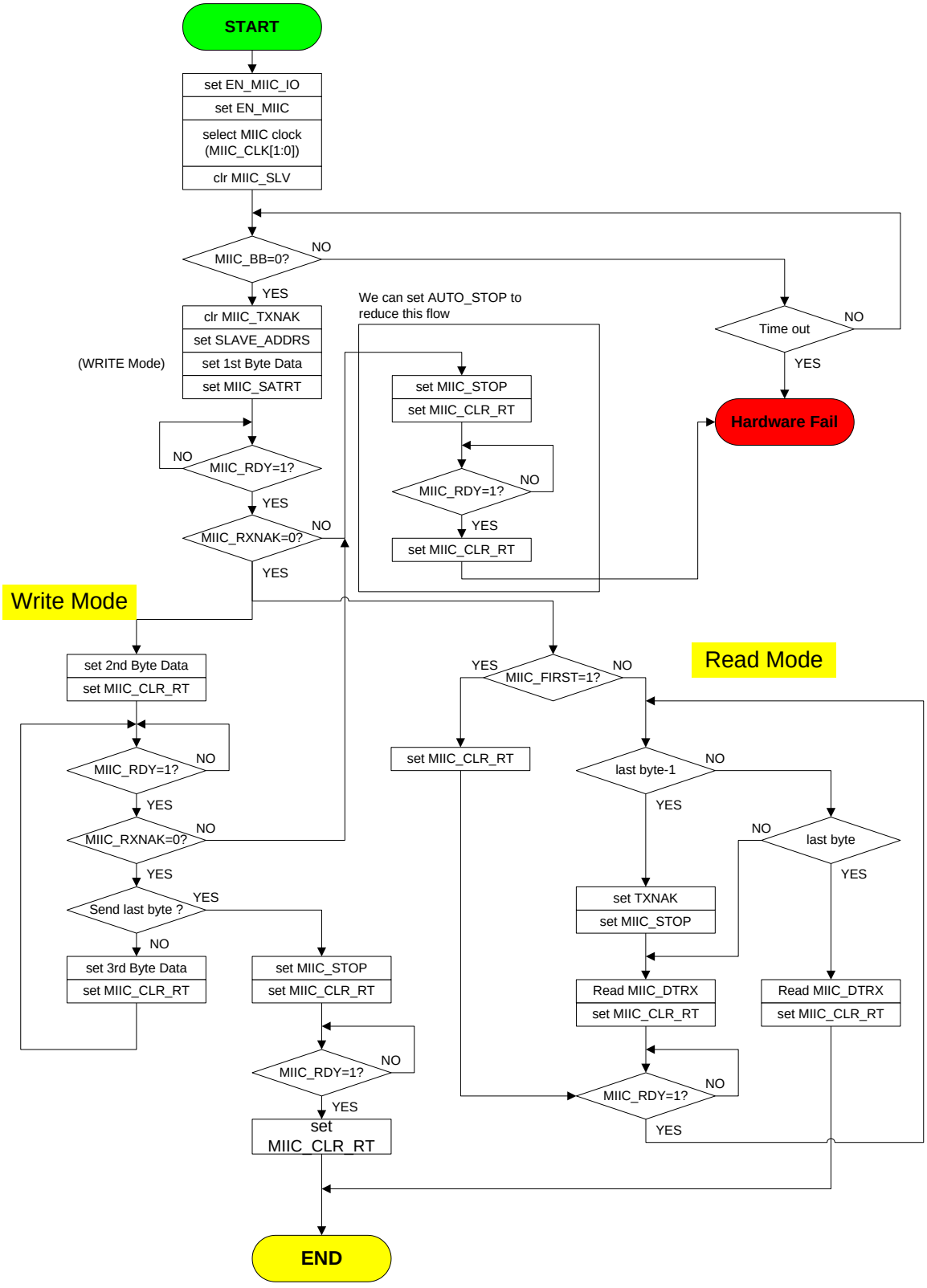
(3) Slave write mode :



(4) Slave read mode :



WT56F116S/108S Master/Slave I²C Data Flow



6.12 Enhanced Timer/Counter

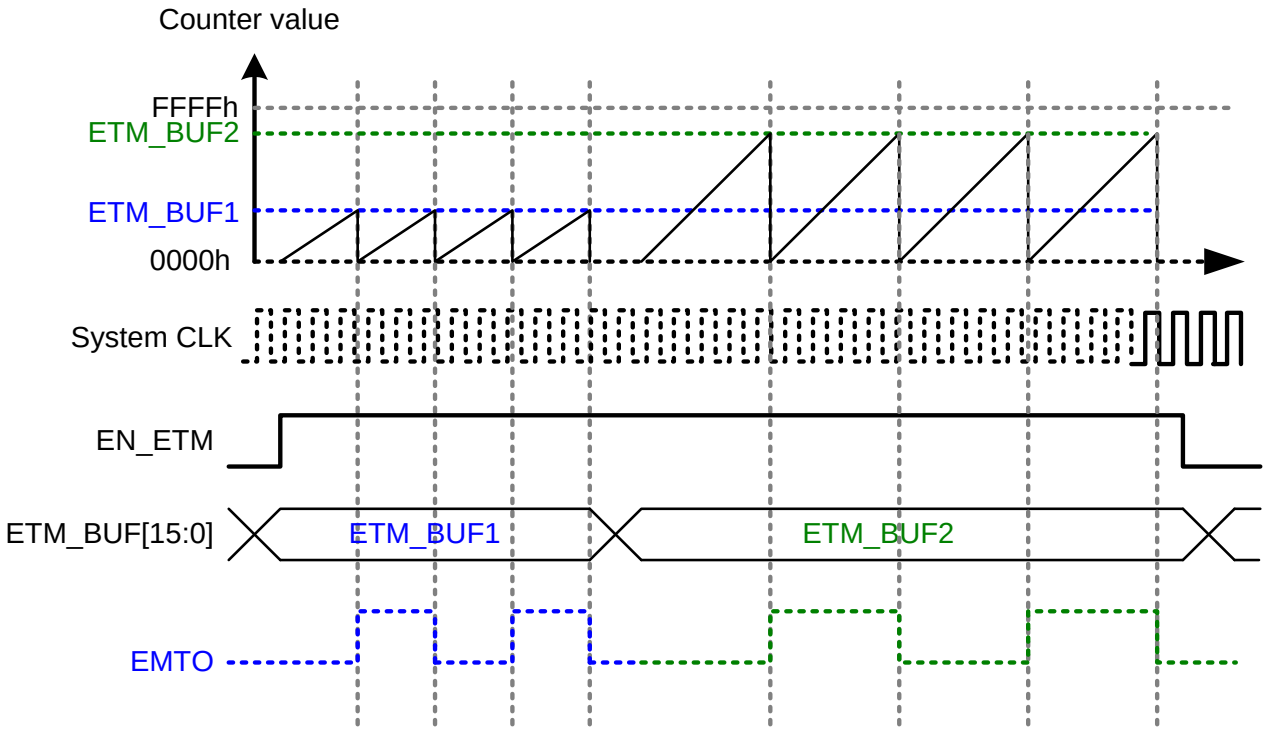
The clock sources of enhanced Timer/Counter are from internal or external clock, and it is determined by register.

The Enhanced Timer/Counter has two operation modes: 1. Compare mode. 2. Capture mode. Furthermore there are three types of Capture Match condition for selection: High-level, Low-level, and Period of Capture mode.

1. Compare mode:

The Enhanced Timer/Counter contains one 16-bit Counter and one 16-bit enhanced Buffer (ETM_BUF[15:0]). When enable the Enhanced Timer/Counter (EN_ETM = 1) and set as the compare mode (ETM_MODE[1:0] = 00), the counter will start counts according to the clock sources, and an interrupt will occur once the data of the counter matches the data of the enhanced Buffer. Each match will output the trigger of ETMO (general-purpose I/O port A0) and clear the counter value of the internal 16-bit Counter. Please refer to the figure below.

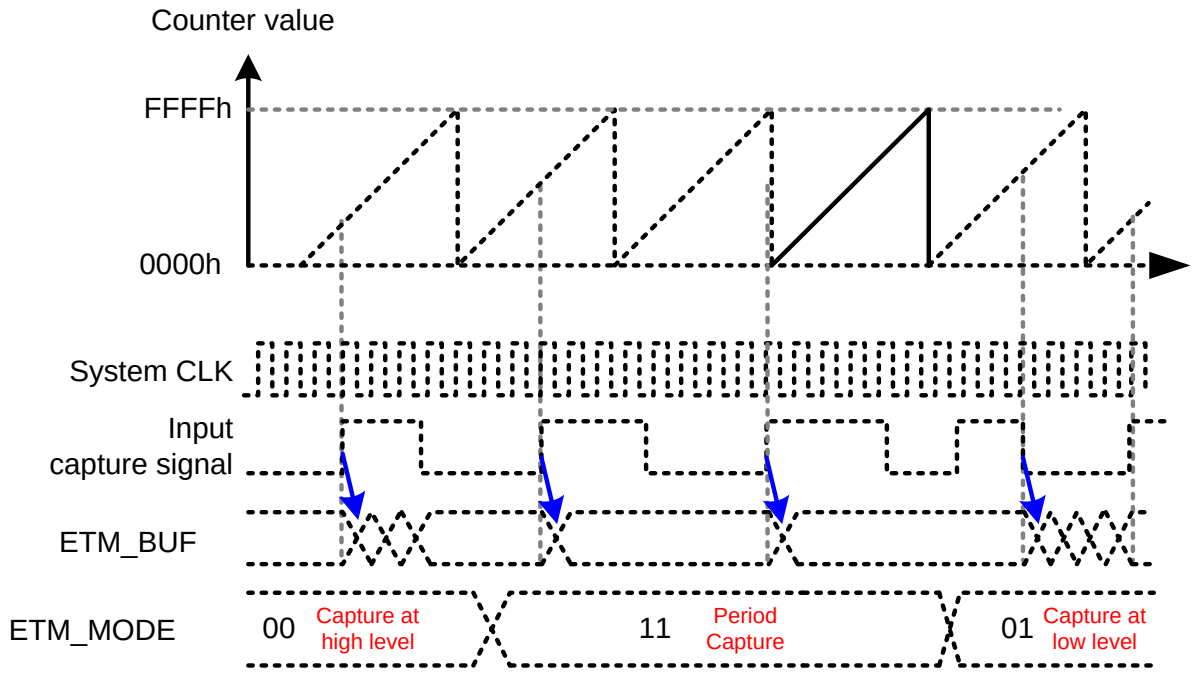
Compare mode operation flow:



2. Capture mode

If the Enhanced Timer/Counter is set as the Capture mode (ETM_MODE[1:0] = 01, 10, 11), and it is enabled (EN_ETM = 1), the capture operation starts. When the input status changes then match with the setting capture condition, the internal 16-bit counter will be cleared and restarts counting, then reload the counter value into 16-bit Buffer (ETM_BUF[15:0]) automatically. At the same time, the software can read the counter value from the Enhanced Timer/Counter Data Buffer Register (register B3H & B4H), and a capture interrupt, capture flag and output ETMO may be generated. Please refer to the figure below.

Capture mode operation flow:



Enhanced Timer/Counter Control Register 1 ETM_CTL1 (XFR: 0xB0) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	RW	R/W	R/W	R/W
Name	EN_ETM	ETM_MODE[1:0]		ETM_SOURCE[2:0]			ETM_CLK_PSCAL[1:0]	

Bit Number	Bit Mnemonic	Description
7	EN_ETM	1: Enable Enhanced Timer/Counter
6-5	ETM_MODE[1:0]	00: Compare mode (SOURCE clock = 12 MHz) 01: capture counting mode, capture the interval of high level 10: capture counting mode, capture the interval of low level 11: capture counting mode, capture the interval period (based on the setting ETM_IN_PSCAL[1:0] to capture)
4-2	ETM_SOURCE[2:0]	Compare Mode: Set clock source prescalers of the internal 16-bit Counter 000: Enhanced Timer/Counter clock source = SOURCE clock 001: Enhanced Timer/Counter clock source = SOURCE clock/12

Bit Number	Bit Mnemonic	Description
		100: Enhanced Timer/Counter input external clock source channel = ETMIA (GPIOA7) 101: Enhanced Timer/Counter input external clock source channel = ETMIB (GPIOA3) 110: Enhanced Timer/Counter input external clock source channel = ETMIC (GPIOA1) Other value: Enhanced Timer/Counter clock source = SOURCE clock Capture mode: Set Enhanced Timer/Counter clock source & capture channel 000: Enhanced Timer/Counter clock source = SOURCE clock，capture channel is ETMIA (GPIOA7) 001: Enhanced Timer/Counter clock source = SOURCE clock，capture channel is ETMIB (GPIOA3) 010: Enhanced Timer/Counter clock source = SOURCE clock，capture channel is ETMIC (GPIOA1) 100: Enhanced Timer/Counter clock source = SOURCE clock / 12，capture channel is ETMIA (GPIOA7) 101: Enhanced Timer/Counter clock source = SOURCE clock / 12，capture channel is ETMIB (GPIOA3) 110: Enhanced Timer/Counter clock source = SOURCE clock / 12，capture channel is ETMIC (GPIOA1)
1-0	ETM_IN_PSCAL [1:0]	Set input channel period prescaler 00: input period/1 01: input period/4 10: input period/8 11: input period/16

Note: As the external clock source of the Enhanced Timer/Counter is one of GPIOA7, GPIA3, or GPIOA1, please set the complex function of GPIO as GPIO, and input floating.

Enhanced Timer/Counter Interrupt Register ETM_INT (XFR: 0xB2) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	W	R	R	R	-
Name	EN_CAPINT	EN_OVRINT	EN_CMPINT	CLR_FLAG	CAPF	OVRF	CPMF	Reserved

Bit Number	Bit Mnemonic	Description
7	EN_CAPINT	1: Enable input capture interrupt 0: Disable input capture interrupt
6	EN_OVRINT	1: Enable overflow interrupt 0: Disable overflow interrupt
5	EN_CMPINT	1: Enable Compare Match Interrupt 0: Disable Compare Match Interrupt
4	CLR_FLAG	1: Clear all Enhanced Timer/Counter flags
3	CAPF	Input capture flag
2	OVRF	Overflow flag When an overflow occurred in internal 16-bit counter, OVRF = 1
1	CPMF	Compare match flag When internal 16-bit counter has the same value as ETM_BUF,

Bit Number	Bit Mnemonic	Description
		CPMF = 1
0	Reserved	-

-: unimplemented.

Enhanced Timer/Counter Data Buffer Low Bytes Register ETM_BUF[7:0] (XFR: 0xB3) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	ETM_BUF[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	ETM_BUF[7:0]	Paired with ETM_BUF[15:8] to form a 16-bit counter value Read: In Capture mode, the counter value of the captured input signal Write: In Compare mode, as the compare value to compare with the internal 16-bit counter

Enhanced Timer/Counter Data Buffer High Bytes Register ETM_BUF [15:8] (XFR: 0xB4) **Reset Value: 80h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	ETM_BUF[15:8]							

Bit Number	Bit Mnemonic	Description
7-0	ETM_BUF[15:8]	Paired with ETM_BUF[7:0] to form a 16-bit counter value Read: In Capture mode, the counter value of the captured input signal Write: In Compare mode, as the compare value to compare with the internal 16-bit counter

Note: In Capture mode, ETM_BUF[15:8] and ETM_BUF[7:0] form a 16-bit counter value, and the counter value should be incremented by one to be the actual counter value in application.

Explanation 1:

Due to internal capture source goes through the filter, the pulse width of input signal high level and low level must be greater than the width of four SYSTEM Clocks.

Explanation 2:

ETM_IN_PSCAL[1:0] = 00: Select Capture Input Source 1 cycle, then the Capture effective Resolution is 1 / 12 MHz / 1 = 83.333 ns

ETM_IN_PSCAL[1:0] = 11: Select Capture Input Source 16 cycles, then the Capture effective Resolution is 1 / 12 MHz / 16 = 5.208 ns

When select Capture 16 cycles allow the enhanced Timer/Counter to get more significant digits, to reduce capture error.

6.13 Analog/Digital Converter (ADC)

WT56F116S/108S has a built-in 16-channel 10-bit Analog/Digital Converter, and it also provides two conversion modes (Single, Voltage Compare) and four conversion rate (2 MHz, 1 MHz, 500 kHz, and 125 kHz) for selection. Reference Voltage Source VREF has two options: Power Voltage VDD, External Reference Voltage VREF.

The conversion time of A/D Converter is 14us (sampled time 4 us + conversion time 10 us) based on the conversion rate of 1 MHz.

Single Mode:

Turn on the A/D converter power (XFR: 0xD0 ADC_CTL, and ADC_PD = 0), and set the ADC_SINGLE_CVT = 1, then the A/D conversion starts. When ADC_SINGLE_CVT = 0, the conversion is finished. When conversion is completed, the conversion data will be updated and an interrupt will generate (ADFINSH_FLG = 1). If ADC convert finish Interrupt is enabled (EN_ADFINSH_INT = 1), the ADC interrupt will generate.

Voltage Compare Mode:

When turn on the A/D converter power (XFR: 0xD0 ADC_CTL, and ADC Control Register ADC_PD = 0), and activate the Compare function (EN_ADC_CMP = 1), the conversion data of Analog input compare 10-bit setting of XFR: 0xD4 & 0xD5 (ADC_CMP_V). When the corresponding digital value of the voltage analog input is greater than (ADC_BIG = 0) or smaller than (ADC_BIG = 1) the setting value of ADC_CMP_V register, the ADC interrupt will occur. The Voltage Compare function of A/D Converter module works as a wakeup source. In addition, working together with XFR: 0xD1 ADC_SEL & ADCMP_TM, it can define ADC turn on time for power-saving purpose.

ADC Control Register ADC_CTL (XFR: 0xD0) **Reset Value: 80h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	-	R/W
Name	ADC_PD	ADC_SINGLE_CVT	ADC_CNTNU_CVT	ADC_AUTO_CVT	EN_ADC_CMP	EN_ADC_FLT	Reserved	ADC_BIG

Bit Number	Bit Mnemonic	Description
7	ADC_PD	Analog/Digital Converter Power Control 1: turn off ADC power 0: turn on ADC power
6	ADC_SINGLE_CVT	ADC start convert bit (single convert mode) 1: ADC start convert 1 => 0: convert finished (hardware will be auto-cleared as “0”)
5	ADC_CNTNU_CVT	1: Enable ADC continuous convert (continuous convert mode) 0: Disable ADC continuous convert
4	ADC_AUTO_CVT	1: Enable ADC auto convert one time based on Watch Timer event WTMR_SLT[2:0] (Timer Compare mode)
3	EN_ADC_CMP	1: Enable ADC compare mode (Voltage compare mode)
2	EN_ADC_FLT	1: Enable ADC filter (need to wait for 332 nsec) 0: Disable filter function
1	Reserved	-
0	ADC_BIG	ADC data compare flag 1: the data set when Vin < ADC_CMP_V[9:0] 0: the data set when Vin > ADC_CMP_V[9:0] Vin: the channel select by EN_AD[3:0]

Note: Only one converting mode is allowed to enable the ADC at the same time, otherwise ADC may work abnormally.

ADC Set Control Register ADC_SEL (XFR: 0xD1) **Reset Value: 40h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	-	-	-	R/W	R/W
Name	ADC_CLK_SEL[1:0]		ADCMP_TM	Reserved			ADC_VREF_SEL	

Bit Number	Bit Mnemonic	Description
7-6	ADC_CLK_SEL[1:0]	ADC convert time clock base 00: 1 MHz 01: 500 kHz 10: 125 kHz 11: 31.25 kHz
5	ADCMP_TM	1: ADC is based on Watch Timer to turn on 32us Voltage compare function at every 32ms for power-saving purpose 0: ADC always compare time
4-2	Reserved	-
1-0	ADC_VREF_SEL	ADC reference voltage selection 00: from VDD 01: from VREF pin 10: VREF refers to Internal 1.23V or 2.44V Bandgap (refers to BGP_VOL_SLT)

-: unimplemented.

Note: When reference voltage of DAC is Bandgap, the calibration value should be filled in the Special Function Register (XFR: 0xF9).
EX: Move flash memory XDATA 0x0E06 to XFR_0xF9 register.

ADC Interrupt Control Register ADC_INT (XFR: 0xD2) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	-	-	R	R	R	-
Name	EN_ADCMP_INT	EN_ADFINSH_INT	Reserved		ADCMP_FLG	ADFINSH_FLG	ADCMP_FLG	Reserved

Bit Number	Bit Mnemonic	Description
7	EN_ADCMP_INT	1: Enable ADC Compare Interrupt 0: Disable ADC Compare Interrupt
6	EN_ADFINSH_INT	1: Enable ADC Convert Finish Interrupt 0: Disable ADC Convert Finish Interrupt
5-4	Reserved	-
3	ADCMP_EDG_FLG	ADC Compare Mode Flag. If the condition selected by ADC_BIG bit in ADC Control Register is met, ADCMP_EDG_FLG = 1.
2	ADFINSH_FLG	ADC Finish Interrupt Flag (If the ADC finished convert in single mode, ADFINSH_FLG = 1)
1	ADCMP_FLG	ADC Data Compare Flag 1: When Vin > ADC_CMP_V[9:0] 0: When Vin < ADC_CMP_V[9:0] Vin: Channel selected by EN_AD[3:0]
0	Reserved	-

-: unimplemented.

Note: When read AD_DATA[9:0], the hardware will auto clear the ADCMP_EDG_FLG & ADFINSH_FLG flag.

ADC Channel Control Register ADC_ENCH (XFR: 0xD3) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				EN_AD[3:0]			

Bit Number	Bit Mnemonic	Description
7-4	Reserved	-
3-0	EN_AD[3:0]	Analog/Digital Channel Selection 0000: Select Channel CH0 0001: Select Channel CH1 0010: Select Channel CH2 0011: Select Channel CH3 0100: Select Channel CH4 0101: Select Channel CH5 0110: Select Channel CH6 0111: Select Channel CH7 1000: Select Channel CH8 1001: Select Channel CH9 1010: Select Channel CH10 1011: Select Channel CH11 1100: Select Channel CH12 1101: Select Channel CH13 1110: Select Channel CH14 1111: Select Channel CH15

-: unimplemented.

ADC Voltage Compare Data High Bytes Register ADC_CMP_V[9:2] (XFR: 0xD4) **Reset Value: 80h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	ADC_CMP_V[9:2]							

Bit Number	Bit Mnemonic	Description
7-0	ADC_CMP_V[9:2]	ADC_CMP_V[9:2] Compare Voltage Setting, paired with ADC_CMP_V[1:0] to form a 10-bit data

ADC Voltage Compare Data Low Bytes Register ADC_CMP_V[1:0] (XFR: 0xD5) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	-	R/W	R/W
Name	Reserved						ADC_CMP_V[1:0]	

Bit Number	Bit Mnemonic	Description
7-2	Reserved	-
1-0	ADC_CMP_V[1:0]	ADC_CMP_V[1:0] Compare Voltage setting, paired with ADC_CMP_V[9:2] to form a 10-bit data

-: unimplemented.

ADC Converted Data High Bytes Register AD_DATA[9:2] (XFR: 0xD6) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	AD_DATA[9:2]							

Bit Number	Bit Mnemonic	Description
7-0	AD_DATA[9:2]	AD_DATA[9:2] converted data setting, paired with AD_DATA[1:0] to form a 10-bit data

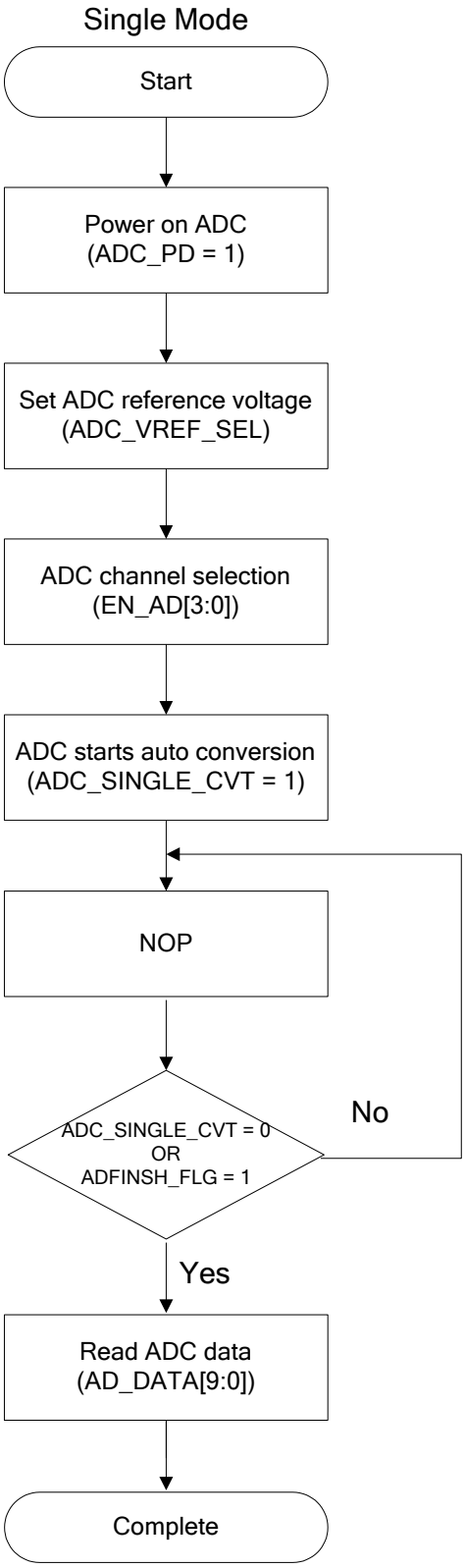
ADC Converted Data Low Bytes Register AD_DATA[1:0] (XFR: 0xD7) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	-	R	R
Name	Reserved						AD_DATA[1:0]	

Bit Number	Bit Mnemonic	Description
7-2	Reserved	-
1-0	AD_DATA[1:0]	AD_DATA[1:0] converted data setting, paired with AD_DATA[9:2] to form a 10-bit data

-: unimplemented.

The setting of Enabling Analog/Digital Converter converted Data procedure:



6.14 Digital/Analog Converter (DAC)

WT56F116S/108S has a built-in 1-channel 10-bit Digital /Analog Converter, and it's a fixed converter rate.

- Reference Voltage Source VREF has four options: Power Voltage VDD, External Reference Voltage VREF, Built-in 1.23V/2.44V Bandgap reference voltage
- The conversion time of D/A Converter is 20us (sampled time 10 us + conversion time 10 us)
- Sink current 300uA

DAC Control Register DAC_CTL (XFR: 0xD8) **Reset Value: 80h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	-	-	-	-	-
Name	DAC_PD	DAC_VREF_SEL		Reserved				

Bit Number	Bit Mnemonic	Description
7	DAC_PD	Digital/Analog Converter Power Control 1: turn off DAC power 0: turn on DAC power
6-5	DAC_VREF_SEL	ADC reference voltage selection 00: from VDD 01: from VREF pin 10: VREF refers to Internal 1.23V or 2.44V Bandgap (refers to BGP_VOL_SLT)
4-0	Reserved	-

Note: When reference voltage of DAC is Bandgap, the calibration value should be filled in the Special Function Register (XFR: 0xF9).
EX: Move flash memory XDATA 0x0E06 to XFR_0xF9 register.

DAC Converted Data High Bytes Register DAC_DATA[9:2] (XFR: 0xD9) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	DAC_DATA[9:2]							

Bit Number	Bit Mnemonic	Description
7-0	DAC_DATA[9:2]	DAC_DATA[9:2] converted data setting, paired with DAC_DATA[1:0] to form a 10-bit data

-: unimplemented.

DAC Converted Data Low Bytes Register DAC_DATA[1:0] (XFR: 0xDA) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	-	R	R
Name	Reserved						DAC_DATA[1:0]	

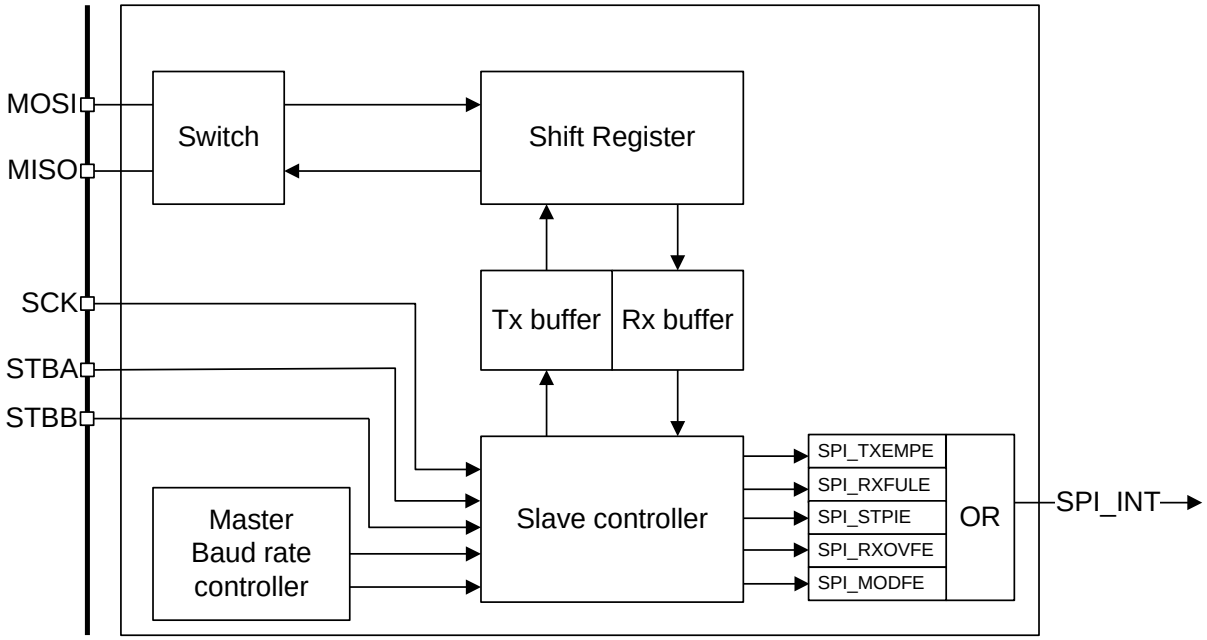
Bit Number	Bit Mnemonic	Description
7-2	Reserved	-
1-0	DAC_DATA[1:0]	DAC_DATA[1:0] converted data setting, paired with DAC_DATA[9:2] to form a 10-bit data

-: unimplemented.

6.15 Serial Peripheral Interface (SPI)

SPI is a synchronous serial interface, allows master to communicate with slave, supports full duplex data transmission, and also supports 3-wire or 4-wire communication.

- SPI supports: Master and Slave mode
- Transmitted serial data can select LSB or MSB being transmitted first
- SPI serial interface transmission speed, frequency range: 6 MHz ~ 23.4375 kHz (Bit Rate)



SPI communication uses four pins, as described below.

MOSI: In Master mode data output; in Slave mode data input.

MISO: In Master mode data input; in Slave mode data output.

SCK: In Master mode clock output; in Slave mode clock input for data synchronization.

STB: In Master mode as output; in Slave mode as input.

In Master mode, as the I/O port to enable Slave:

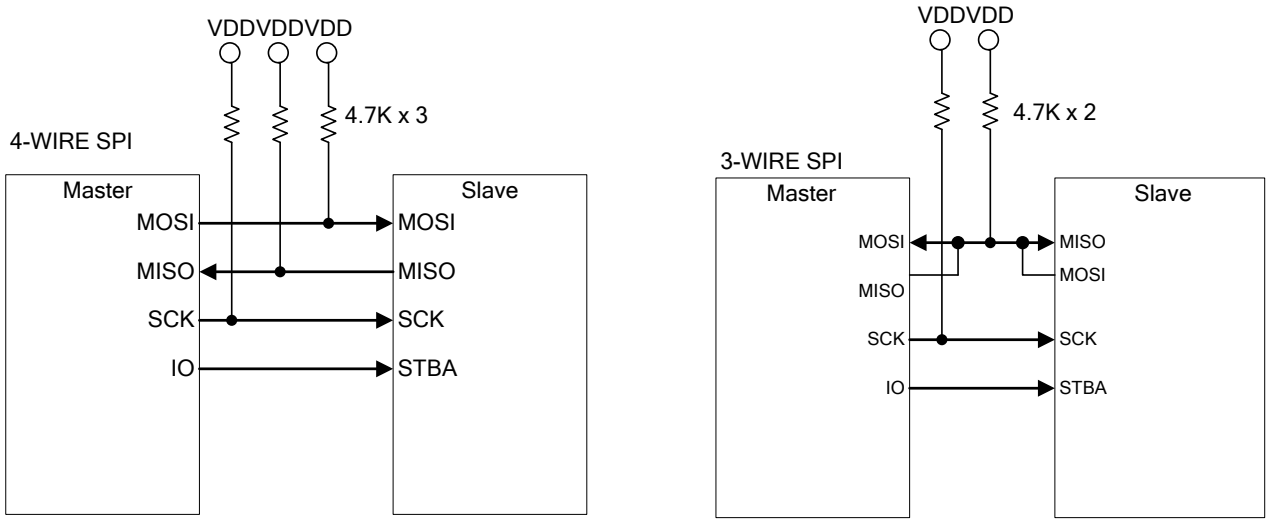
STB = 1: Master disables Slave

STB = 0: Master enables Slave

When use the SPI serial interface, the SPI related pins must be set as output or input status by software, as illustrated below:

4-wire SPI	Master mode	Slave mode	Remarks
MOSI (GPIOE5)	Output	Input	
MISO (GPIOE6)	Input	Output	
SCK (GPIOE7)	Output	Input	
STB (GPIOE4)	Output	Input	

4-wire and 3-wire SPI connection diagram:



SPI Control Register 1 SPI_CTL1 (XFR: 0xC0) **Reset Value: 0x00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	-	R/W	-	-
Name	SPI_EN	SPI_MASTER	SPI_CPOL	SPI_CPHA	Reserved	SPI_LSBFE	Reserved	

Bit Number	Bit Mnemonic	Description
7	SPI_EN	1: Enable SPI module 0: Disable SPI module
6	SPI_MASTER	SPI Master/Slave mode selection 1: SPI as Master mode 0: SPI as Slave mode
5	SPI_CPOL	SPI Clock Polarity bit selection 1: Active-low clock selection 0: Active-high clock selection
4	SPI_CPHA	SPI Clock Phase bit selection 1: Sampling data at even edge of input SPI clock 0: Sampling data at odd edge of input SPI clock
3	Reserved	-
2	SPI_LSBFE	LSB-First Enable 1: Data is transferred LSB bit first 0: Data is transferred MSB bit first
1-0	Reserved	-

-: unimplemented.

***SPI serial interface modes are composed of SPI_CPOL and SPI_CPHA, and are classified into four modes as listed below.**

SPI_CPOL	SPI_CPHA	Receive data by	Transmit data by	SPI Mode
0	0	Positive-edge trigger	Negative-edge trigger	0
0	1	Negative-edge trigger	Positive-edge trigger	1
1	0	Negative-edge trigger	Negative-edge trigger	2
1	0	Positive-edge trigger	Positive-edge trigger	3

*** Transmit and Receive methods can also refer to "SPI Mode Timing" section that will be described later.**

SPI Control Register 2 SPI_CTL2 (XFR: 0xC1) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	-	-	-	-
Name	SPI_RXONLY	SPI_DFBYP	SPI_DLY[1:0]		Reserved			

Bit Number	Bit Mnemonic	Description
7	SPI_RXONLY	SPI Receive Enable Bit (Master mode use only) 1: Enable SPI Receive mode
6	SPI_DFBYP	Input Digital Filter Bypass Enable Bit (Slave mode use only) 1: Enable Digital Filter
5-4	SPI_DLY[1:0]	Master SPI byte delay control 00: No delay 01: delay 1 byte 10: delay 2 bytes 11: delay 3 bytes
3-0	Reserved	-

-: unimplemented.

SPI Interrupt Control Register SPI_INT (XFR: 0xC2) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	-	-	-
Name	SPI_TXEMPE	SPI_RXFULE	SPI_STPIE	SPI_RXOVFE	SPI_MODFE	Reserved		

Bit Number	Bit Mnemonic	Description
7	SPI_TXEMPE	1: Enable SPI Tx data buffer empty interrupt
6	SPI_RXFULE	1: Enable SPI Rx data buffer full interrupt
5	SPI_STPIE	1: Enable SPI Tx sequence finish interrupt
4	SPI_RXOVFE	1: Enable SPI Rx data buffer overflow interrupt
3	SPI_MODFE	1: Enable SPI mode fault Interrupt (Slave mode only)
2-0	Reserved	-

-: unimplemented.

SPI Interrupt Clear Register SPI_CLR (XFR: 0xC3) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	-	-	-	-
Name	CLR_TXEMP	CLR_RXFUL	CLR_STPIF	CLR_RXOVF	Reserved			

Bit Number	Bit Mnemonic	Description
7	CLR_TXEMP	1: Clear SPI Tx data buffer empty interrupt flag
6	CLR_RXFUL	1: Clear SPI Rx data buffer interrupt flag
5	CLR_STPIF	1: Clear SPI sequence full finish interrupt flag
4	CLR_RXOVF	1: Clear SPI Rx data buffer overflow flag
3-0	Reserved	-

-: unimplemented.

SPI Flag Register SPI_FLG (XFR: 0xC4) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	-	-
Name	SPI_TXEMP	SPI_RXFUL	SPI_STPIF	SPI_RXOVF	SPI_MODF	SPI_BUSY	Reserved	

Bit Number	Bit Mnemonic	Description
7	SPI_TXEMP	SPI transmit data buffer empty flag *1 1: SPI Tx data buffer is empty
6	SPI_RXFUL	SPI receive data buffer full flag 1: SPI Rx data buffer is full
5	SPI_STPIF	SPI Transmit/Receive data finish flag (SS pin goes high) 1: SPI Tx/Rx finish
4	SPI_RXOVF	SPI Rx data buffer overflow flag *2 1: SPI receive data buffer overflows
3	SPI_MODF	SPI mode failure status flag (only allowed in Slave mode) *3 1: SPI mode failure
2	SPI_BUSY	SPI Busy status flag *4 1: SPI busy status
1-0	Reserved	-

-: unimplemented.

*1. The firmware must confirm that only when SPI_TXEMP = 1, then the next data is allowed to be written into SPI Transmit Buffer Register (SPI_RXBUF[7:0]).

*2. The SPI_RXOVF flag can be cleared by reading SPI Receive Buffer Register (SPI_RXBUF[7:0]).

*3. The SPI_MODF flag can be cleared by enabling SPI serial interface module.

*4. SPI_BUSY flag is the status of the WT56F116S/108S internal pin, and it can monitor if SPI is finished or not.

SPI Bit Rate Setting Register SPI_BRS[7:0] (XFR: 0xC5) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	SPI_BRS[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	SPI_BRS[7:0]	SPI Bit rate selection (SPI maximum clock = mcu_clk/2) SPI Bit rate = mcu_clk/(SPI_BRS[7:0]+1) x 2 If mcu_clk = 12 MHz, SPI_BRS[7:0] = 0, SPI Bit Rate is 6 MHz SPI_BRS[7:0] = 1, SPI Bit Rate is 3 MHz … SPI_BRS[7:0] = 255, SPI Bit Rate is 23.4375 kHz

SPI Transmit Buffer Register SPI_TXBUF[7:0] (XFR: 0xC6) **Reset Value: FFh**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	SPI_TXBUF[7:0]							

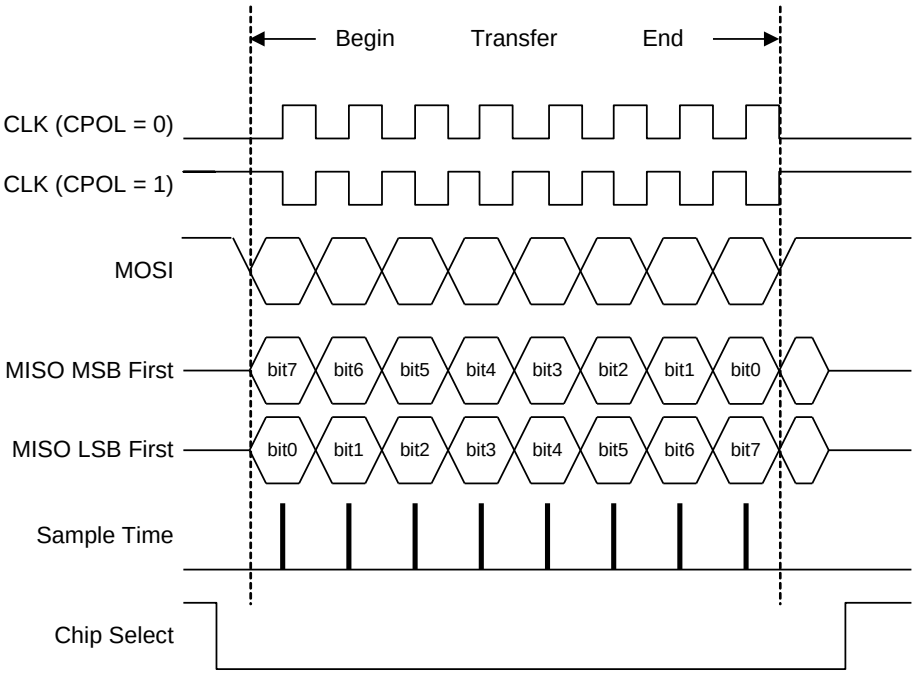
Bit Number	Bit Mnemonic	Description
7-0	SPI_TXBUF[7:0]	SPI Transmit Data Buffer

SPI Receive Buffer Register SPI_RXBUF[7:0] (XFR: 0xC7) **Reset Value: 00h**

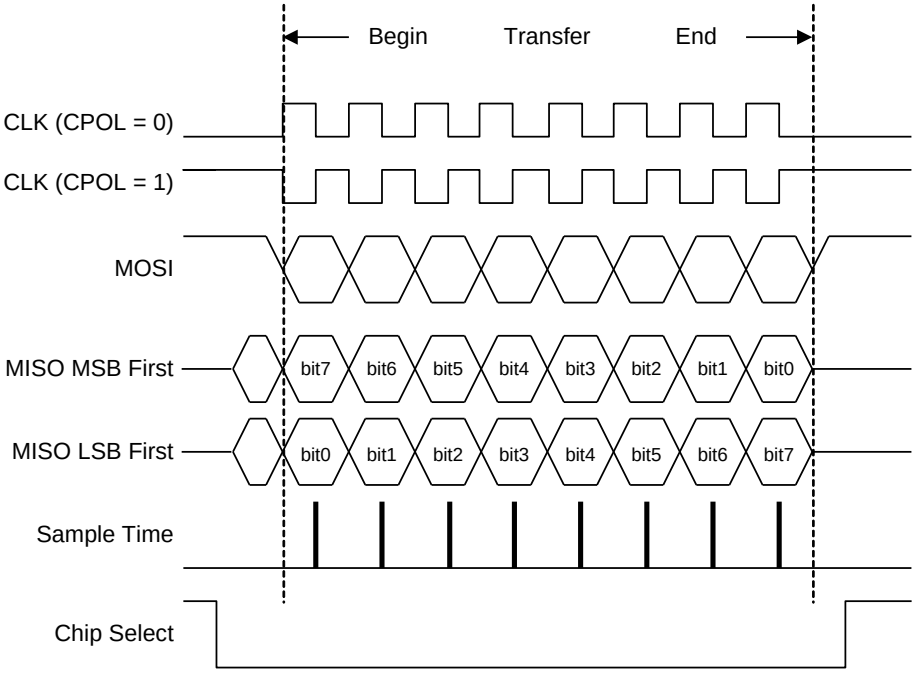
Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	SPI_RXBUF[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	SPI_RXBUF[7:0]	SPI Receive Data Buffer

SPI Mode Timing



(CPHA = 0)



(CPHA = 1)

6.16 Low Voltage Reset (LVR)

WT56F116S/108S has a built-in Low Voltage Reset circuitry which can detect the supply voltage falls below the minimum specified operating voltage then generates a Reset, and it stops when the supply voltage is higher than the detection voltage V_{LVR}.

- The Enable and Disable function of Low Voltage Reset are controlled by the software
- Low Voltage Reset level is about 1.50V ± 10%. Please refer to section 7.8 “Electrical Characteristics” for more details.

Low Voltage Reset Control Register LVR_CTL (XFR: 0x0C) Reset Value: A6h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	-	R/W	R/W
Name	Reserved					Reserved	DIS_FBR	LVR_PD

Bit Number	Bit Mnemonic	Description
7-3	Reserved	Must equal to “11001”, otherwise LVR_PD cannot be written into
2	Reserved	-
1	DIS_FBR	1: Disable built-in Oscillator Feedback Resistor 0: Enable built-in Oscillator Feedback Resistor
0	LVR_PD	1: Power down “Low Voltage Reset” 0: Enable “Low Voltage Reset”

6.17 Low Voltage Detection (LVD)

WT56F116S/108S has a built-in Low Voltage Detection circuitry which can detect the supply voltage falls below the minimum specified operating voltage then generates an Interrupt.

- The Enable and Disable function of Low Voltage Detection are controlled by the software
- Low Voltage Detection level provides 8-level of voltage for selection: 2.00V, 2.25V, 2.50V, 2.75V, 3.00V, 3.25V, 3.50V or 3.75V

Low Voltage Detection Control Register LVD_CTL (XFR: 0x02) **Reset Value: A6h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	**R/W**	**R**	**R/W**	**R/W**	**R/W**	R/W	R/W	R/W
Name	**LVD_PD**	**LVD_CMP**	**LVD_LVL[2:0]**			LVD_RST_PD	LCD_RST_LVL[1:0]	

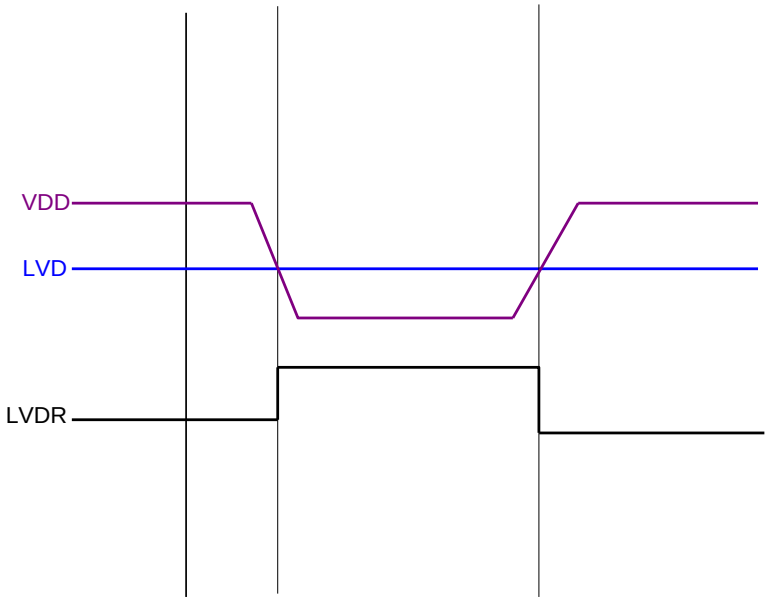
Bit Number	Bit Mnemonic	Description
7	LVD_PD	1: Power down Low Voltage Detection 0: Turn on Low Voltage Detection
6	LVD_CMP	Low Voltage Detection Compared Result 1: Power Voltage < setting Low Voltage Detection voltage 0: Power Voltage > setting Low Voltage Detection voltage
5-3	LVD_LVL[2:0]	Low Voltage Detection Range: 000: 2.00V 001: 2.25V 010: 2.50V 011: 2.75V 100: 3.00V 101: 3.25V 110: 3.50V 111: 3.75V

Note: The voltage range of Low Voltage Detection has great tolerance. Please refer to section 7.8 Electrical Characteristics for more details.

6.18 Low Voltage Detection Reset (LVDR)

WT56F116S/108S has a built-in Low Voltage Detection circuitry which can detect the supply voltage falls below the minimum specified operating voltage then generates a Reset.

- The Enable & Disable function of Low Voltage Detection Reset are controlled by the software
- Low Voltage Detection level provides 4-level of voltage for selection: 2.00V, 2.50V, 3.00V, 3.5V



Low Voltage Detection Control Register LVD_CTL (XFR: 0x02) **Reset Value: A6h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R	R/W	R/W	R/W	**R/W**	**R/W**	**R/W**
Name	LVD_PD	LVD_CMP	LVD_LVL[2:0]			**LVD_RST_PD**	**LCD_RST_LVL[1:0]**	

Bit Number	Bit Mnemonic	Description
2	LVD_RST_PD	1: Power down Low Voltage Detection Reset 0: Turn on Low Voltage Detection Reset
1-0	LVD_RST_LVL[1:0]	Low Voltage Detection Reset Range: 00: 2.00V 01: 2.50V 10: 3.00V 11: 3.50V

Note: The voltage range of Low Voltage Detection Reset has great tolerance. Please refer to Section 7.8 "Electrical Characteristics" for more details.

Reset Flag Register RESET_FLG (XFR: 0x03) **Reset Value: 01h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	R	R	R	R	R	R	R
Name	CLR_RST_FLG	PC_OVL_RST_FLG	ISP_RST_FLG	WDT_RST_FLG	NRST_FLG	LVD_RST_FLG	LVR_RST_FLG	POR_RST_FLG

Bit Number	Bit Mnemonic	Description
7	CLR_RST_FLG	1: Clear all Reset Flag
6	PC_OVL_RST_FLG	1: Reset source is from program counter overflow
5	ISP_RST_FLG	1: Reset source is from ISP
4	WDT_RST_FLG	1: Reset source is from Watchdog
3	NRST_FLG	1: Reset source is from External Reset pin
2	LVD_RST_FLG	1: Reset source is from Low Voltage Detection Reset
1	LVR_RST_FLG	1: Reset source is from Low Voltage Reset
0	POR_RST_FLG	1: Reset source is from External Power Reset

Note: For more details, please refer to Section 5.7 “Reset”.

6.19 Emulated E²PROM

The WT56F116S/108S can use Flash PROM space to emulate E²PROM.
WT56F116S storage address locates from 0x3800 ~ 0x3BFF (1024 Bytes)
WT56F108S storage address locates from 0x1800 ~ 0x1BFF (1024 Bytes)

E²PROM Enable Register 1 EER_EN1[3:0] (XFR: 0xE0) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	W	W	W	W
Name	Reserved				EER_EN1[3:0]			

Bit Number	Bit Mnemonic	Description
7-4	Reserved	-
3-0	EER_EN1[3:0]	When EER_EN1[3:0] = '1010' and EER_EN2[3:0] = '0101', the E²PROM function is enabled.

-: unimplemented.

E²PROM Enable Register 2 EER_EN2[3:0] (XFR: 0xE1) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	W	W	W	W
Name	Reserved				EER_EN2[3:0]			

Bit Number	Bit Mnemonic	Description
7-4	Reserved	-
3-0	EER_EN2[3:0]	When EER_EN2[3:0] = '0101' and EER_EN1[3:0] = '1010', the E²PROM function is enabled.

-: unimplemented.

E²PROM Address Low Bytes Register EER_ADDR[7:0] (XFR: 0xE2) **Reset Value: FFh**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Name	EER_ADDR[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	EER_ADDR[7:0]	EER_ADDR[7:0] address setting, paired with EER_ADDR[10:8] to form a 11-bit address

E²PROM Address High Bytes Register EER_ADDR[11:8] (XFR: 0xE3) **Reset Value: 07h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	-	R/W	R/W	R/W
Name	Reserved					EER_ADDR[10:8]		

Bit Number	Bit Mnemonic	Description
7-3	Reserved	-
2-0	EER_ADDR[10:8]	EEP_ADDR[10:8] address setting, paired with EER_ADDR[7:0] to form a 11-bit address

-: unimplemented.

E²PROM Control Register EER_TCTL[3:0] (XFR: 0xE4) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	W	W	R/W	R/W	R/W	R/W
Name	Reserved		EER_ERASE	EER_PROG	EER_TCTL[3:0]			

Bit Number	Bit Mnemonic	Description
7-6	Reserved	-
5	EER_ERASE	1: E²PROM proceeds ERASE (1024 Bytes) /page 0: Did not proceed ERASE
4	EER_PROG	1: Programming function program (1 Byte) (auto-cleared as 0) 0: No program *hold time = 80.08us~84.5us@12MHz,EER_TCTL = default
3-0	EER_TCTL[3:0]	E²PROM Erase/Program Timing (See "Notes")

-: unimplemented.

E²PROM Break Register EER_BRK (XFR: 0xE6) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	R/W	R/W	-	-	-	-
Name	EER_BRK_ERASE_EN	EER_BRK_PROG_EN	EER_BRK_ERASE_FLAG	EER_BRK_PROG_FLAG	Reserved			

Bit Number	Bit Mnemonic	Description
7	EER_BRK_ERASE_EN	1: Enable E²PROM erasing can be break by interrupt events
6	EER_BRK_PROG_EN	1: Enable E²PROM programming can be break by interrupt events.
5	EER_BRK_ERASE_FLAG	1: Erase operation Break Flag CPU writes 0 to clear this flag
4	EER_BRK_PROG_FLAG	1: Programming operation Break Flag CPU writes 0 to clear this flag
3-0	Reserved	Must be set as 0

E²PROM Data Register EER_DAT0[7:0] (XFR: 0xE8) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	W	W	W	W	W	W	W	W
Name	EER_DATA[7:0]							

Bit Number	Bit Mnemonic	Description
7-0	EER_DATA[7:0]	E²PROM Data Register

Note:

1 · In programming E²PROM, all functions are halt state of 8052.
2 · It takes 500 μ sec to programming E²PROM while working at 3.3V.
Default value: EER_TCTL[3:0] = 1000. The programming time of 1 Byte = 80 μ sec ~ 85 μ sec.
The erasing time of 1 Bank (256 Bytes) = 32 msec ~ 36 msec.

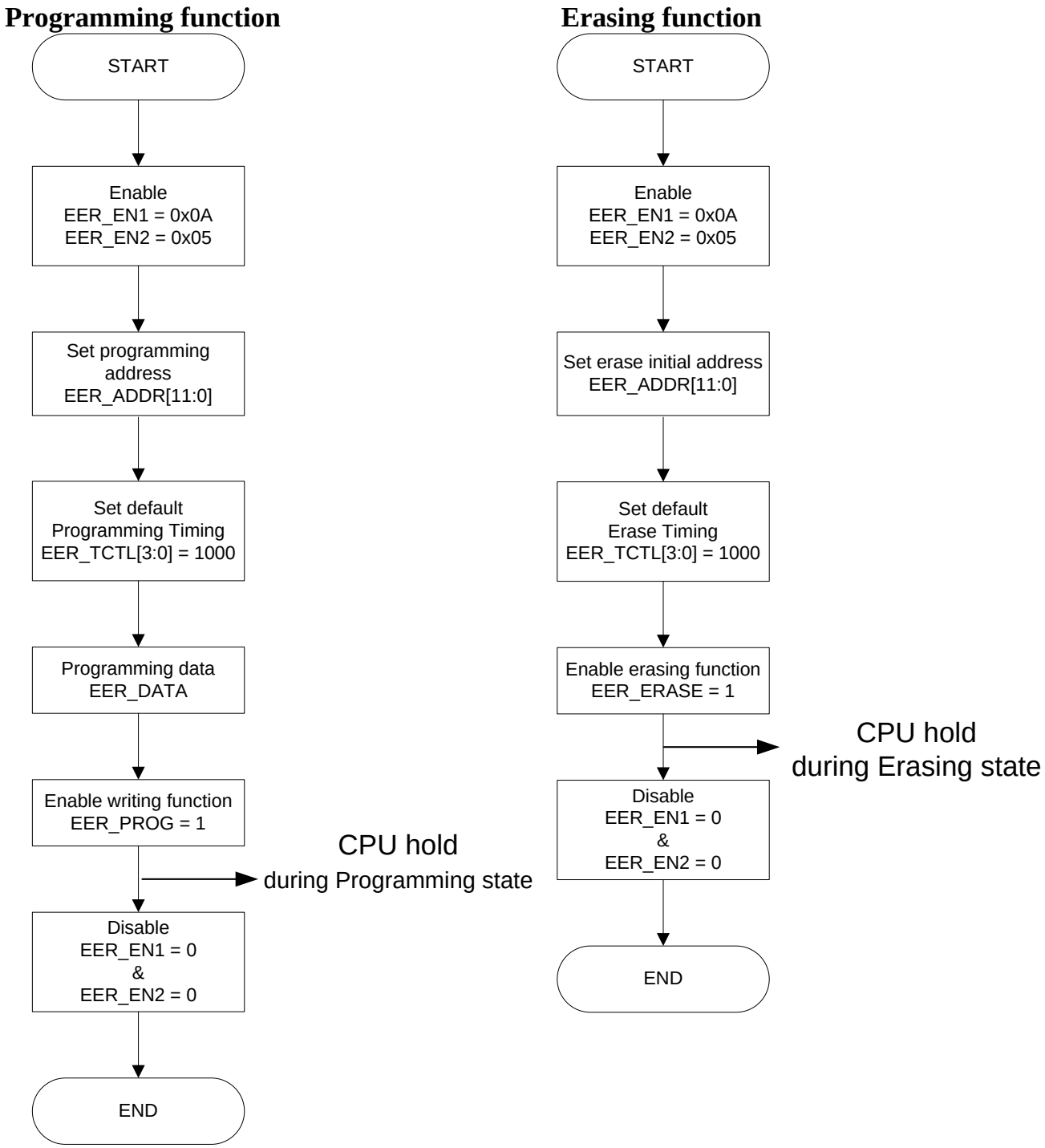
WT56F116S E²PROM Address Setting (1K Flash size)

Flash address	EER_ADDR[10:8]	EER_ADDR[7:0]	Erase Range
0x3800	000	0x00~0xFF	0x3800~ 0x3BFF

WT56F108S E²PROM Address Setting (1K Flash size)

Flash address	EER_ADDR[10:8]	EER_ADDR[7:0]	Erase Range
0x1800	000	0x00~0xFF	0x1800~ 0x1BFF

E^{2}PROM Enable Flow chart:



6.20 Code Option

Code Block located in the last eight bytes of Flash ROM for storing customer ID and IC configuration with address listed as the following table.

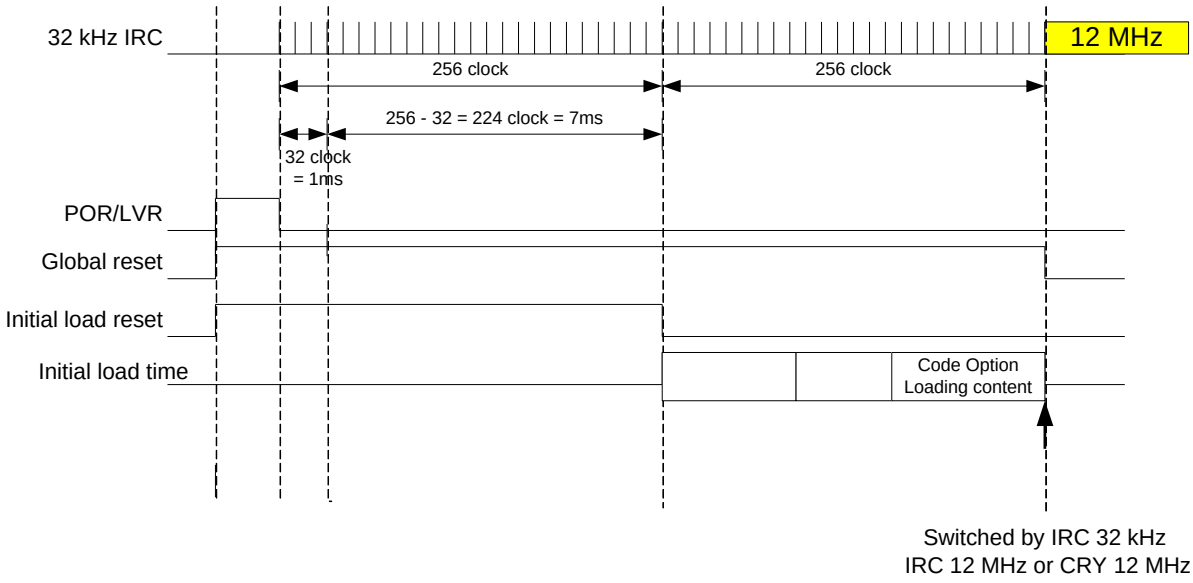
If this function is not enabled, please reserve the space of these eight bytes, and fill it with 0xFF.

If the function is enabled, WT56F116S/108S will auto reload the code option at each reset. Please refer to the Sequence Diagram as listed below.

Address	Bit Number	Description
3FF8H/1FF8H	7-0	= AFH, enable Code Option = FFH, disable Code Option Default value 0xFF
3FF9H/1FF9H	7-0	Customer ID 1, mapping to XFR: CSM_ID1 = 0x0D[7:0] Default value 0xFF: code can be assigned by SWUT ISP software programming
3FFAH/1FFAH	7-0	Customer ID 2, mapping to XFR: CSM_ID2 = 0x0E[7:0] Default value 0xFF: code can be assigned by SWUT ISP software programming
3FFBH/1FFBH	7-0	Customer ID 3, mapping to XFR: CSM_ID3 = 0x0F[7:0] Default value 0xFF: code can be assigned by SWUT ISP software programming
3FFCH/1FFCH	7-0	Flash memory content protection: it is an individual setting, and will not be turned off even if Code Option is disabled. = 5AH flash memory cannot be read = A5H flash memory cannot be written into Default value 0xFF: Flash can read/write
General Purpose I/O Complex Function Options Setting:		
3FFDH/1FFDH	7-6	Reserved
	5-4	Mapping to XFR: GPF1_FUN_SLT = 0x2DH[3:2] 00: GPIO (default) 01: COM1, LCD common 1 10: MOSCO2 (served as the Crystal oscillator output pin of path 2, will auto define GPIOF0 as the crystal oscillator input pin (MOSC12) instead of GPIO function) 11: P05
	3	Mapping to XFR: GPA5_FUN_SLT = 0x25H[2] 1: MOSCI1 served as the Crystal oscillator input pin of path 1, will auto define GPIOA4DH as the crystal oscillator output pin (MOSCO1) instead of GPIO function) 0: GPIO (default), and it also set GPIOA4DH as GPIO function
	2	Mapping to XFR: LVD_RST_PD = 02H[2] 1: Turn off low voltage detection reset power (default) 0: Turn on low voltage detection reset power
	1-0	Mapping to XFR: LVD_RST_LVL[1:0] = 02H[1:0] 00: 2.0V 01: 2.5V 10: 3.0V (default) 11: 3.5V
Oscillator Initialization and Driving Ability Options Setting:		
3FFEH/1FFEH	7	Reserved
	6	Mapping to XFR: DIS_FBR = 0CH[1]

Address	Bit Number	Description
		1: Disable built-in oscillator feedback resistor 0: Enable built-in oscillator feedback resistor
	5-4	Mapping to XFR: SOURCE_CLK_SLT[1:0] = 0x05H[3:2]; SOURCE clock 00: Internal 12 MHz RC oscillator (default) 01: External DC ~ 16 MHz crystal oscillator 10: Internal 32 kHz RC oscillator 11: Reserved
	3-1	Mapping to XFR: CRY_12M_DR[1:0] = 0x08H[3:1]; external crystal oscillator driving ability selection 000: Select 32.768 kHz crystal oscillator (VDD > 2.4V) 001: Select 32.768 kHz crystal oscillator 010: Select 100 kHz crystal oscillator 100: Select 1 MHz ~ 12 MHz crystal oscillator (default) 110: Select 12 MHz ~ 24 MHz crystal oscillator
	0	Mapping to XFR: SLT_CRYSTAL = 0x08H[0]; crystal oscillator input pins selection 1: the crystal oscillator input pins of path 2, MOSCI2 (GPIOF0), MOSCO2 (GPIOF1) 0: the crystal oscillator input pins of path 1, MOSCI1 (GPIOA5), MOSCO1 (GPIOA4) (default)
All Oscillator Power Switch Options Setting:		
3FFFH/1FFFH	7-5	Reserved
	4	Mapping to XFR: IRC_12M_PD1 = 0x07H[4] 1: Turn off partial power of internal 12 MHz RC oscillator 0: Turn on partial power of internal 12 MHz RC oscillator (default)
	3	Mapping to XFR: IRC_12M_PD2 = 0x07H[3] 1: Turn off all power of internal 12 MHz RC oscillator 0: Turn on all power of internal 12 MHz RC oscillator (default)
	2	Reserved
	1	Mapping to XFR: CRY_12M_PD = 0x07H[1] 1: Turn off external 12 MHz ~ 32 kHz crystal oscillator (default) 0: Turn on external 12 MHz ~ 32 kHz crystal oscillator
	0	Reserved

Note: Code option setting would be overwritten by program setting, it is recommended to use the program to set the code option. Please refer to the next page for code option setting examples and code example program.



WT56F116S/108S Code Option example:

```
;-------------------------------------------------------------------------------
; This Code : CodeOption116S.A51 is for WT56F116S Code Option Setting
;-------------------------------------------------------------------------------

; Version: 1.00 >>@2016-05-15, First Version

;-------------------------------------------------------------------------------
;;=============================================================================================
#define OPTION_ON               1
#define OPTION_OFF              0
;;Default OFF Code Option
#define WT56F116S_CODE_OPTION     OPTION_ON


    #if(WT56F116S_CODE_OPTION==OPTION_ON)
    ;;Load Code option switch
    CSEG       AT 0x3FF8
    DB     10101111B  ;;0xAx: load code option

    ;;Customer ID 1 default 0xFF
    CSEG       AT 0x3FF9
    DB     11111111B
    ;;Customer ID 2 default 0xFF
      CSEG       AT 0x3FFA
    DB     11111111B
    ;;Customer ID 3 default 0xFF
      CSEG       AT 0x3FFB
    DB     11111111B

    ;;Flash Protect Read/Write
      CSEG       AT 0x3FFC
    ;;Flash memory content protection:
    ;;default 0xFF select no protection MCU can read/write
    ;;bit7-0 = 5AH flash memory cannot be read
    ;;bit7-0 = A5H flash memory cannot be written into(For one time programming)
    DB     11111111B
    ;DB         01011010B  ;; 0x5A
    ;DB         10100101B  ;; 0xA5

    ;;Crystal GPIO setting
      CSEG       AT 0x3FFD
    ;;bit[5:4] = (main crystal2: GPF1_FUN_SLT= 2DH[3:2] = 2'b10)
            ;;00: GPIO
            ;;01: COM1
            ;;10: MOSC 2 (2nd Crystal oscillator pad)
            ;;11: P05
    ;;bit[3]     = (main crystal1: GPA5_FUN_SLT= 25H[2] )
            ;;0: GPIO
            ;;1: MOSC1 (1st Crystal oscillator PAD)
    ;;bit[2]     = (LVD_RST_PD=02H[2])
            ;;0: LVD reset enable
            ;;1: LVD Reset power down
    ;;bit[1:0] = (LVD_RST_LVL[1:0]=02H[1:0])
            ;;11: 3.50v
            ;;10: 3.00v
```

```
            ;;01: 2.50v
            ;;00: 2.00v

    DB      00000010B   ;;default
;   DB      00001000B   ;;    test using OSC1 pin, bit[3] = 1
;   DB      00100000B   ;;    test using OSC2 pin, bit[5:4] = 10

    ;;Source Clock and Crystal drive setting
      CSEG      AT 0x3FFE
    ;;bit7  NC     default 0
    ;; bit6 : DIS_FBR= 0CH[1]
            ;;1: Disable built-in Feedback Resistor
            ;;0: Enable built-in Feedback Resistor
    ;; bit[5:4]:MAIN_CLK_SLT[1:0]=05H[3:2]
            ;;00: main clock = Internal RC 12Mhz OSC (default)
            ;;01: main clock = Crystal 12Mhz OSC
            ;;10: main clock = Internal RC 32KHz OSC(initial)
            ;;11: Reserved
    ;; bit[3:1]:CRY_12M_DR[2:0]=08H[3:1]
            ;;000: 32KHz power saving(>2.4v)
            ;;001: 32KHz
            ;;010: 100KHz
            ;;100: 1MHz – 12MHz (default)
            ;;110: 12MHz – 16MHz
    ;; bit0 : SLT_CRYSTAL select main crystal 1 or 2=08H[0]
            ;;0 : select crystal 1
            ;;1 : select crystal 2

    DB      00001100B  ;; default
;   DB      00011000B  ;;    Ext 12MHz and using OSC1 pin
;   DB      00011001B  ;;    Ext 12MHz and using OSC2 pin

    ;;Crystal Power setting
      CSEG      AT 0x3FFF
    ;;bit7  NC     default 0
    ;;bit6  NC     default 0
    ;;bit5  NC     default 0
    ;;bit4  Mapping to XFR: IRC_12M_PD1 0x07H[4] default turn on
        ;;1: turn off partial power of internal 12 MHz RC oscillator
        ;;0: turn on partial power of internal 12 MHz RC oscillator
    ;;bit3  Mapping to XFR: IRC_12M_PD2 0x07H[3] default turn on
        ;;1: turn off all power of internal 12 MHz RC oscillator
        ;;0: turn on all power of internal 12 MHz RC oscillator
    ;;bit2  NC     default 0

    ;;bit1  Mapping to XFR: CRY_12M_PD 0x07H[1] default turn off
        ;;1: Turn off external 1 MHz ~ 24 MHz crystal oscillator
        ;;0: Turn on external 1 MHz ~ 24 MHz crystal oscillator
    ;;bit0  NC     default 0
    DB      00000000B  ;; default
;   DB      00000000B  ;;    turn ON Ext 12MHz

    #else
    CSEG      AT 0x3FF8
    DB      11111111B
    CSEG      AT 0x3FF9
    DB      11111111B
```

```
CSEG    AT 0x3FFA
DB   11111111B
CSEG    AT 0x3FFB
DB   11111111B
CSEG    AT 0x3FFC
DB   11111111B
CSEG    AT 0x3FFD
DB   11111111B
CSEG    AT 0x3FFE
DB   11111111B
CSEG    AT 0x3FFF
DB   11111111B
#endif
```

Customer ID1 ~ 3 mapped to the Customer Code Registers 1 ~ 3, please refer to the following customer code register.

Customer Code Register 1 CSTM_ID1 (XFR: 0x0D) **Reset Value: FFh**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	CSTM_ID1							

Bit Number	Bit Mnemonic	Description
7-0	CSTM_ID1	Customer code, paired with CSTM_ID2 and CSTM_ID3, 3 bytes in total.

Customer Code Register 2 CSTM_ID2 (XFR: 0x0E) **Reset Value: FFh**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	CSTM_ID2							

Bit Number	Bit Mnemonic	Description
7-0	CSTM_ID2	Customer code, paired with CSTM_ID3 and CSTM_ID1, 3 bytes in total.

Customer Code Register 3 CSTM_ID3 (XFR: 0x0F) **Reset Value: FFh**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R	R	R	R	R	R	R	R
Name	CSTM_ID3							

Bit Number	Bit Mnemonic	Description
7-0	CSTM_ID3	Customer code, paired with CSTM_ID1 and CSTM_ID2, 3 bytes in total.

Note: WT56F116S/108S code option provides one byte (8 bits) available for customer to set, reading are taken in by the program storage area after each Reset.

The following registers is described in the previous section, and now is set for the Code Option registers mapped in the General-purpose I/O Complex Function options, including the option settings of the crystal oscillator pins and crystal oscillator sources.

0x25, 0x2D, 0x05, 0x07, 0x08 registers again described as below.

General-purpose I/O Port A Complex Function Setting Register 1 GPIOA_FUN1 (XFR: 0x25) **Reset Value: 00h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	R/W	R/W	-	-	-	R/W	-	-
Name	GPA7_FUN_SLT[1:0]		Reserved			GPA5_FUN_SLT	Reserved	

Bit Number	Bit Mnemonic	Description
7-6	GPA7_FUN_SLT[1:0]	Set GPIOA7DH complex function 00: GPIO/ETMIA/IRQ0 (default) 01: RXA, RX of path A of UART (select RXA, and auto define GPIOA6DH as TXA)

Bit Number	Bit Mnemonic	Description
		10: Reserved 11: P00 output/input (mapping to 8052 P0.0)
5-3	Reserved	-
2	GPA5_FUN_SLT	Set GPIOA5DH complex function 1: MOSCI1 (served as the Crystal oscillator input pins of path 1, and will auto define GPIOA4DH as the oscillator output pin (MOSCO1) instead of GPIO function) 0: GPIO (default), and meanwhile GPIOA4DH will be set as GPIO function. Code option can be selected by 6.20 Code Option
1-0	Reserved	-

-: unimplemented.

Notes: The setting of using External Crystal Oscillator as SOURCE clock (using Crystal Oscillator as the input pins of path 1):

1. **Select Crystal Oscillator as the input pins of path 1: MOSCI1, MOSCO1. (XFR 0x08 SLT_CRYSTAL = 0)**
2. **Set GPIOA5 and GPIOA4 as Input port. (XFR 0x10 GPIOA_OE[5:4])**
3. **GPIOA5 and GPIOA4 disable internal pull high resistor. If enable pull high resistor will result in oscillator outputs unstable frequency. (XFR 0x1E GPIOA_PHN[5:4])**
4. **Set GPIOA5 and GPIOA4 as Crystal Oscillator pins. (XFR 0x25 GPA5_FUN_SLT)**
5. **Set the driving ability of External Main Crystal Oscillator. (XFR 0x08 CRY_12M_DR[2:0])**
6. **Power on External Crystal Oscillator switch. (XFR 0x07 CRY_12M_PD)**
7. **Switch SOURCE clock to External Crystal Oscillator. (XFR 0x05 SOURCE_CLK_SLT[1:0])**

General-purpose I/O port F Complex Function Setting Register2 GPIOF_FUN2 (XFR: 0x2D) Reset Value: 00h

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	R/W	-	R/W	R/W	R/W	-	R/W
Name	Reserved	GPF3_FUN_SLT	Reserved	GPF2_FUN_SLT	GPF1_FUN_SLT[1:0]		Reserved	GPF0_FUN_SLT

Bit Number	Bit Mnemonic	Description
7	Reserved	-
6	GPF3_FUN_SLT	Set GPIOF3 complex function 1: COM3, LCD Common 3 0: GPIO (default)
5	Reserved	-
4	GPF2_FUN_SLT	Set GPIOF2 complex function 1: COM2, LCD Common 2 0: GPIO (default)
3-2	GPF1_FUN_SLT[1:0]	Set GPIOF1 complex function 00: GPIO (default) 01: COM1, LCD common 1 10: MOSCO2, served as the Crystal oscillator output pin of path 2, and will auto define GPIOF0 as the crystal oscillator input pins (MOSCI2) instead of GPIO function.

Bit Number	Bit Mnemonic	Description
		11: reserved Default value can be selected by 6.20 Code Option
1	Reserved	-
0	GPF0_FUN_SLT	Set GPIOF0 complex function 1: COM0, LCD Common 0 0: GPIO (default)

-: unimplemented.

Notes: The setting of using External Crystal Oscillator as SOURCE clock (using Crystal Oscillator as the input pins of path 2):

1. **Select Crystal Oscillator as the input pins of path 2: MOSCI2, MOSCO2. (XFR 0x08 SLT_CRYSTAL = 1)**
2. **Set GPIOF1 and GPIOF0 as Input port. (XFR 0x15 GPIOF_OE[1:0])**
3. **GPIOF1 and GPIOF0 disable internal pull high resistor. If enable pull high resistor will result in oscillator outputs unstable frequency. (XFR 0x20 GPIOF_PHN)**
4. **Set GPIOF1 and GPIOF0 as Crystal Oscillator pin. (XFR 0x2D GPF1_FUN_SLT[1:0])**
5. **Set the driving ability of External Main Crystal Oscillator. (XFR 0x08 CRY_12M_DR[2:0])**
6. **Power on External Crystal Oscillator switch. (XFR 0x07 CRY_12M_PD)**
7. **Switch SOURCE clock to External Crystal Oscillator. (XFR 0x05 SOURCE_CLK_SLT[1:0])**

System Clock Source Control Register SOURCE_CLK_SLT (XFR: 0x05) **Reset Value: A0h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				SOURCE_CLK_SLT[1:0]		MCU_CLK_SLT[1:0]	

Bit Number	Bit Mnemonic	Description
7-4	-	Must be equal to “1010”, otherwise bit [3:0] cannot be written into.
3-2	SOURCE_CLK_SLT[1:0]	Select SOURCE clock sources 00: internal 12 MHz RC oscillator (default) 01: external DC ~ 16 MHz crystal oscillator 10: internal 32 kHz RC oscillator 11: reserved Default value can be selected by section 6.20 Code Option
1-0	MCU_CLK_SLT[1:0]	MCU clock setting 00: MCU clock and System clock = SOURCE clock 01: MCU clock and System clock = SOURCE clock /2 (default) 10: MCU clock and System clock = SOURCE clock /4 11: MCU clock and System clock = SOURCE clock /12

-: unimplemented.

Clock Source Control Register IRC_12M_PD (XFR: 0x07) **Reset Value: A2h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	R/W	R/W	R/W	R/W	-
Name	Reserved			IRC_12M_PD1	IRC_12M_PD2	IRC_32K_PD	CRY_12M_PD	Reserved

Bit Number	Bit Mnemonic	Description
7-5	-	Must be equal to “101”, otherwise bit[4:0] cannot be written into
4	IRC_12M_PD1	1: partial internal 12 MHz RC oscillator power is turned off (default value is not off) 0: not off Default value can be selected by section 6.20 Code Option
3	IRC_12M_PD2	1: all internal12 MHz RC oscillator power is turned off (default value is not off) 0: not off Default value can be selected by section 6.20 Code Option
2	IRC_32K_PD	1: internal 32 kHz RC oscillator power is turned off (default value is not off) 0: not off Default value can be selected by section 6.20 Code Option
1	CRY_12M_PD	1: external 12 MHz ~ 32 kHz crystal oscillator power is turned off (default value is off) 0: not off Default value can be selected by section 6.20 Code Option
0	Reserved	-

-: unimplemented.

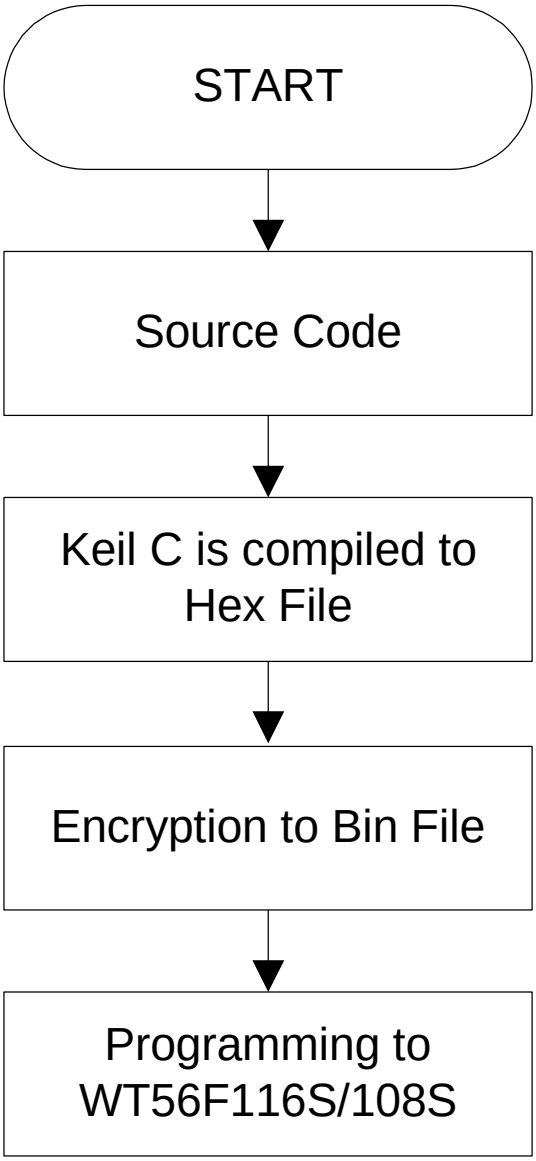
Oscillator Driver Control Register CRY_12M_DR[2:0] (XFR: 0x08) **Reset Value: 58h**

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	-	-	-	-	R/W	R/W	R/W	R/W
Name	Reserved				CRY_12M_DR[2:0]			SLT_CRYSTAL

Bit Number	Bit Mnemonic	Description
7-4	-	Must be equal to “0101”, otherwise, Bit[3:0] cannot be written into
3-1	CRY_12M_DR[2:0]	External oscillator driving ability setting 000: crystal oscillator with frequency of 32.768 kHz (VDD > 2.4V) 001: crystal oscillator with frequency of 32.768 kHz 010: crystal oscillator with frequency of 100 kHz 100: crystal oscillator with frequency of 1 MHz ~ 12 MHz (default) 110: crystal oscillator with frequency of 12 MHz ~ 16 MHz Default value can be selected by section 6.20 Code Option
0	SLT_CRYSTAL	Crystal Oscillator Input pin select 1: the crystal oscillator input pins of path 2: **MOSCI2 (GPIOF0), MOSCO2 (GPIOF1)** 0: the crystal oscillator input pins of path 1: **MOSCI1 (GPIOA5), MOSCO1 (GPIOA4)** Default value can be selected by section 6.20 Code Option

-: unimplemented.

6.21 Read Out Protection



7. Electrical Characteristics

7.1 Absolute Maximum Ratings

Parameter	Symbol	Condition	Range	Units
D.C. Supply Voltage	V_{DD}		-0.3 ~ 6.0	V
Input Voltage	V_I		-0.3 to V_{DD} +0.3	V
Output Voltage	V_O		-0.3 to V_{DD} +0.3	V
Total current source by all GPIO	$\sum I_{OH}$		90@-40℃ ~ +105℃	mA
Total current sink by all GPIO	$\sum I_{OL}$		90@-40℃ ~ +105℃	mA
Ambient Temperature	T_A		-40 ~ 105	℃
Storage Temperature	T_{STG}		-60 ~ 125	℃

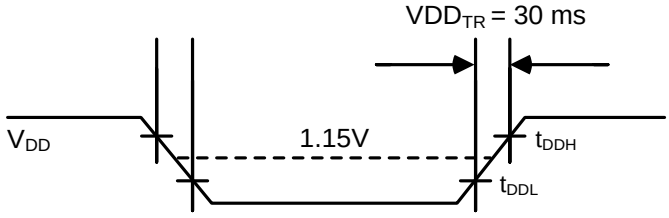
Note: Stresses above those listed may cause permanent damage to the devices.

7.2 Recommended Operating Parameters

Parameter	Symbol	Condition	Specification			Units
			Min	Typ.	Max	
Power Voltage	V_{DD1}	F_{main} = 12/24 MHz	1.8		5.5	V
Bandgap Voltage	V_{BDIE}	V_{DD} = 5V Temp = 25℃		1.23 ±1% 2.44 ±1%		V
Main Frequency	F_{main}	V_{DD} = 1.8V ~ 5.5V		12/24		MHz
Sub Frequency	F_{sub}	V_{DD} = V_{DD}		32.768		kHz
Operating Temperature	T_{OPR}		-40		105	℃
POR (Power on Reset) Level	V_{POR}	At VDD_{TR} = 30 ms, T_A = 25℃ (see Figure below)		1.15		V
VDD Rising Rate(*)	V_{DDTRA}		50			S/V
VDD Falling Rate(*)	V_{DDTFA}		150			S/V

(*): These parameters are presented for design guidance only and not tested or guaranteed.

Power On Reset (POR) Timing



7.3 DC Electrical Characteristics (V_{DD} = 1.8V ~ 5.5V, -40℃ ~ +105℃)

Parameter	Symbol	Condition	Specification			Units
			Min	Typ.	Max	
Schmitt Trigger from Low to High	V_{T+}	V_{DD} = 1.8V ~ 5.5V	0.6 V_{DD}		V_{DD} +0.3	V
Schmitt Trigger from High to Low	V_{T-}	V_{DD} = 1.8V ~ 5.5V			0.2 V_{DD}	V
Output High Voltage (Note)	V_{OH4}	I_{OH} = 4 mA at V_{DD} = 5V GPIOB0 ~ GPIOB3, GPIOC0 ~ GPIOC7, GPIOD0 ~ GPIOD7, GPIOE0 ~ GPIOE7, GPIOF0 ~ GPIOF7, GPIOG0 ~ GPIOG7	V_{DD} -0.4			V
	V_{OH8}	I_{OH} = 8 mA at V_{DD} = 5V GOIOA0 ~ GPIOA7, GPIOB4 ~ GPIOB7	V_{DD} -0.4			
Output Low Voltage (Note)	V_{OL4}	I_{OL} = 4 mA at V_{DD} = 5V GPIOB0 ~ GPIOB3, GPIOC0 ~ GPIOC7, GPIOD0 ~ GPIOD7, GPIOE0 ~ GPIOE7, GPIOF0 ~ GPIOF7, GPIOG0 ~ GPIOG7			V_{SS} +0.4	V
	V_{OL8}	I_{OL} = 8 mA at V_{DD} = 5V GOIOA0 ~ GPIOA7, GPIOB4 ~ GPIOB7			V_{SS} +0.4	
Input Leakage Current(*)	I_{OZ}	V_O = 0V or VDDV		±0.01	±1	μA
Pull-up Resistor	R_{PH}	V_{DD} = 3.3V, V_{PIN} = 0V		33		KΩ
Normal mode at 24 MHz Working Current	I_{VDD24M}	No load on output (V_{DD} = 3.3V, IRC12M on), peripheral off		3.3		mA
Normal mode at 12 MHz Working Current	I_{VDD12M}	No load on output (V_{DD} = 3.3V, IRC12M on), peripheral off		1.7		mA
Normal mode at 6 MHz Working Current	I_{VDD6M}	No load on output (V_{DD} = 3.3V, IRC12M on), peripheral off		1.1		mA
Normal mode at 3 MHz Working Current	I_{VDD3M}	No load on output (V_{DD} = 3.3V, IRC12M on), peripheral off		0.8		mA
Normal mode at 1 MHz Working Current	I_{VDD1M}	No load on output (V_{DD} = 3.3V, IRC12M on), peripheral off		0.6		mA

Parameter	Symbol	Condition	Specification			Units
			Min	Typ.	Max	
Idle mode Working Current	I_{VDDS1}	No load on output (V_{DD} = 3.3V, mcuClk = stop, Peripheral clock = IRC12M), peripheral off		350		μA
Green mode Working Current	I_{VDDS2}	No load on output (V_{DD} = 3.3V, mcuClk = IRC32K, Peripheral clock = IRC32K, LVR off), peripheral off		12		μA
Sleep mode Working Current	I_{VDDS3}	No load on output (V_{DD} = 3.3V, mcuClk = stop, Peripheral clock = stop, LVR off), peripheral off		5		μA
LCD ON Working Current	I_{LCD}	No Load@3V		1.8		μA

(*): These parameters are presented for design guidance only and not tested or guaranteed.

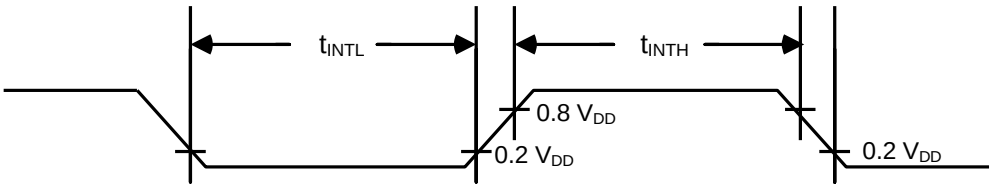
Note: V_{OH4} /V_{OL4} pins maximum sink/source current are 10 mA; V_{OH8} /V_{OL8} pins maximum sink/source current are 20 mA.

7.4 AC Electrical Characteristics (T_A = 25℃)

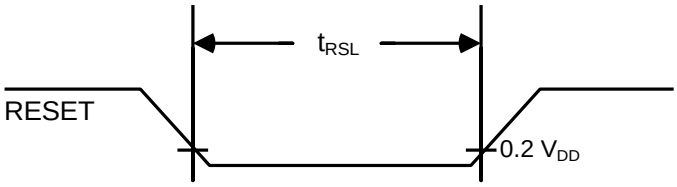
Parameter	Symbol	Pin/condition	Specification			Units
			Min	Typ.	Max	
Main Operation Frequency	F_{MCP}	X_{IN}	0.032		24	MHz
Main Crystal Stabilization Time(*)		V_{DD} = 4.5V ~ 5.5V at 12 MHz			10	ms
		V_{DD} = 1.8V ~ 4.5V at 12 MHz			30	ms
		V_{DD} = 4.5V ~ 5.5V at 32768 Hz		0.5	1	s
		V_{DD} = 1.8V ~ 4.5V at 32768 Hz			10	s
Interrupt Input High, Low Width (IRQx)	t_{INTH}, t_{INTL}	MCU clock = 12 MHz	167			ns
RESET Input Low Width	t_{RSL}	RST_NDF = 1, main clock = 12 MHz	334			ns

(*): These parameters are presented for design guidance only and not tested or guaranteed.

Input Timing for External Interrupts



Input Timing for RESET



7.5 Internal 12/24 MHz RC Oscillator Temperature Tolerance table

Parameter	Symbol	Pin/condition	Specification			Units
			Min	Typ.	Max	
RC Oscillator Frequency	F_{RCH}	V_{DD} = 5V		12		MHz
Ex-factory Frequency Tolerance(*)	$\Delta F_{RCH1}/F_{RCH}$	Without external oscillator for calibrating 25℃		±1		%
		Without external oscillator for calibrating 0℃ ~ 70℃		±2		%
		Without external oscillator for calibrating -40℃ ~ 85℃		±3		%
		Without external oscillator for calibrating -40℃ ~ 125℃		±4		%
		With external oscillator for calibrating -40℃ ~ 125℃			±1	%

(*): These parameters are presented for design guidance only and not tested or guaranteed.

Parameter	Symbol	Pin/condition	Specification			Units
			Min	Typ.	Max	
RC Oscillator Frequency	F_{RCH}	V_{DD} = 5V		24		MHz
Ex-factory Frequency Tolerance(*)	$\Delta F_{RCH1}/F_{RCH}$	Without external oscillator for calibrating 25℃		±1		%
		Without external oscillator for calibrating 0℃ ~ 70℃		±2.5		%
		Without external oscillator for calibrating -40℃ ~ 85℃		±3.5		%
		Without external oscillator for calibrating -40℃ ~ 125℃		±5		%
		With external oscillator for calibrating -40℃ ~ 125℃			±1	%

7.6 A/D Converting Characteristics (T_A = 25℃)

Parameter	Symbol	Pin/condition	Specification			Units
			Min	Typ.	Max	
Resolution				10		bit
Integral Nonlinearity Error (INL)	E_{IL}	AV_{REF} = VDD = 5V		±2		LSB
Differential Nonlinearity Error (DNL)	E_{DL}	AV_{REF} = VDD = 5V		±2		LSB
Offset Error	E_{OFF}	AV_{REF} = VDD = 5V		±2		LSB
Gain Error	E_{GN}	AV_{REF} = VDD = 5V		±2		LSB
Reference Voltage VDD/ExtVref	AV_{REF}	Absolute minimum to ensure 2 LSB accuracy	2		V_{DD}	V
Reference Voltage BandGap = 1.23V (*)				1.23		V
Reference Voltage BandGap = 2.44V (*)				2.44		V
Full-Scale Range	V_{ADCIN}		V_{SS}		V_{REF}	V
Recommended Impedance of Analog Voltage Source	Z_{AiN}				10	KΩ
Vref Input Current	I_{REF}	DAC base on different Vin	10		100	μA
		Comparator			20	μA
Conversion Time	T_{CT}	main clock = 12 MHz	16			ADC_clk
Ground Voltage(*)	AV_{SS}		V_{SS}		V_{SS} +0.3	V
ADC Working Current(*)	I_{ADC}	AV_{REF} = VDD = 5V		0.2		mA
		AV_{REF} = VDD = 5V at Power Down mode			1	μA

(*): These parameters are presented for design guidance only and not tested or guaranteed.

Note: When use BandGap as reference voltage, please pay attention to the operating voltage. Please refer to section 7.7 for more details.

ADC ENOB (Effective number of bits)

Parameter	Pin/condition ADC convert time clock base = 1 MHz	Specification			Units
		Min	Typ.	Max	
ENOB (Effective Number of Bits)	AV_{REF} = VDD = 5V		9		bit
	AV_{REF} = VDD = 4V		8		bit
	AV_{REF} = VDD = 3V		8		bit

Parameter	Pin/condition ADC convert time clock base = 1 MHz	Specification			Units
		Min	Typ.	Max	
	AV_{REF} = VDD = 2V		8		bit
	AV_{REF} = 2.44V (Bandgap) VDD > 2.7V		8		bit
	AV_{REF} = 1.23V (Bandgap) VDD > 2.0V		6		bit

7.7 Bandgap Electrical Characteristic

Parameter	Symbol	Pin/condition	Specification			Units
			Min	Typ.	Max	
Operating Voltage(*)		BGP = 1.23V	1.8		5.5	V
Operating Voltage(*)		BGP = 2.44V	2.7		5.5	V
Operating Temperature(*)			-40		85	℃
Bandgap Voltage	V_{BDIE}	V_{DD} = 5V Temp = 25℃		1.23 ±1% 2.44 ±1%		V
Voltage Variation	V_{BSP}	BGP = 1.23V		5		mV
		BGP = 2.44V		10		mV
Temperature Variation	V_{BTP}	Temp = -40℃~ 85℃ BGP = 1.23V		13		mV
		Temp = -40℃~ 85℃ BGP = 2.44V		25		mV

(*): These parameters are presented for design guidance only and not tested or guaranteed.

Note: Internal reference voltage Bandgap is calibrated out of factory at 2.44V±1% @VDD = 5V, please pay attention to the operating voltage.

7.8 Low Voltage Reset (LVR) & Low Voltage Detection Reset (LVDR) Electrical Characteristics

Parameter	Symbol	Pin/condition	Specification			Units
			Min	Typ.	Max	
LVR Voltage	V_{LVR}	$T_{A=}$ 25℃		1.5		V
LVR/LVDR Working Current	I_{DDPR}	V_{DD} = 5V ±10%		5		μA
LVD & LVDR Response Time				120		μS
Low Voltage Detection Range Tolerance	V_{LCD}			±10		%
Low Voltage Detection Reset Range Tolerance	V_{LVDR}			±10		%

7.9 Thermal Resistance Notice

Parameter	Symbol	Feature	Typ.	Units	Condition
TH01	θ JA	Thermal Resistance (Junction to Air)	57	℃/W	64-pin LQFP package
TH02	θ JC	Thermal Resistance (Junction to Case)	15	℃/W	64-pin LQFP package
TH03	TJMAX	Maximum Junction Temperature	125	℃	64-pin LQFP package

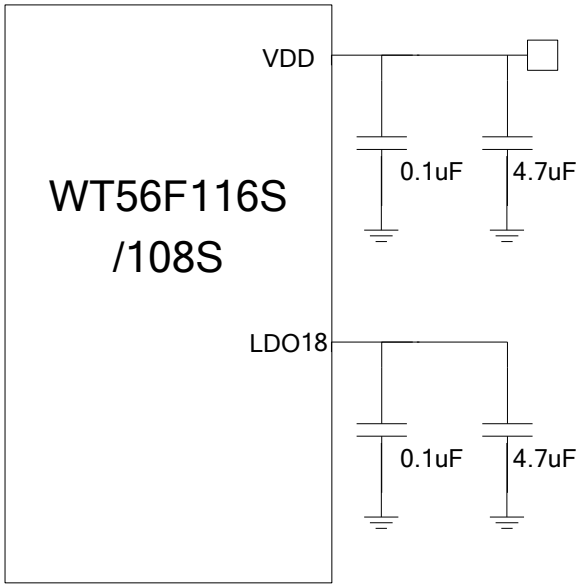
Parameter	Symbol	Feature	Typ.	Units	Condition
TH01	θ JA	Thermal Resistance (Junction to Air)		℃/W	48-pin LQFP package
TH02	θ JC	Thermal Resistance (Junction to Case)		℃/W	48-pin LQFP package
TH03	TJMAX	Maximum Junction Temperature		℃	48-pin LQFP package

Parameter	Symbol	Feature	Typ.	Units	Condition
TH01	θ JA	Thermal Resistance (Junction to Air)		℃/W	28-pin SOP package
TH02	θ JC	Thermal Resistance (Junction to Case)		℃/W	28-pin SOP package
TH03	TJMAX	Maximum Junction Temperature		℃	28-pin SOP package

Parameter	Symbol	Feature	Typ.	Units	Condition
TH01	θ JA	Thermal Resistance (Junction to Air)		℃/W	20-pin SSOP package
TH02	θ JC	Thermal Resistance (Junction to Case)		℃/W	20-pin SSOP package
TH03	TJMAX	Maximum Junction Temperature		℃	20-pin SSOP package

8. Application Circuits

8.1 Power Supply



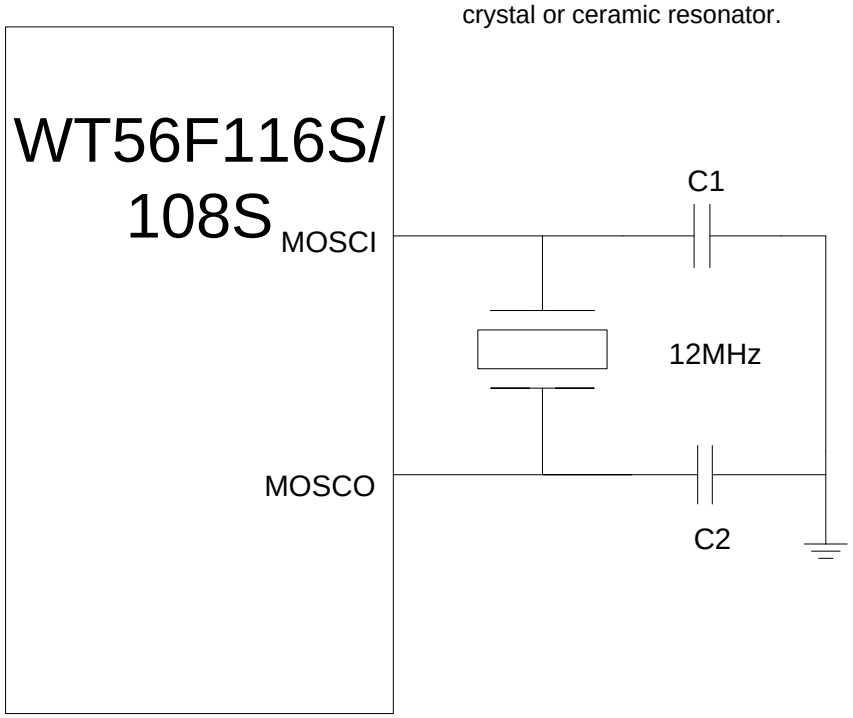
8.2 Oscillator Circuits

8.2.1 External 12/24 MHz Crystal Oscillator

Example

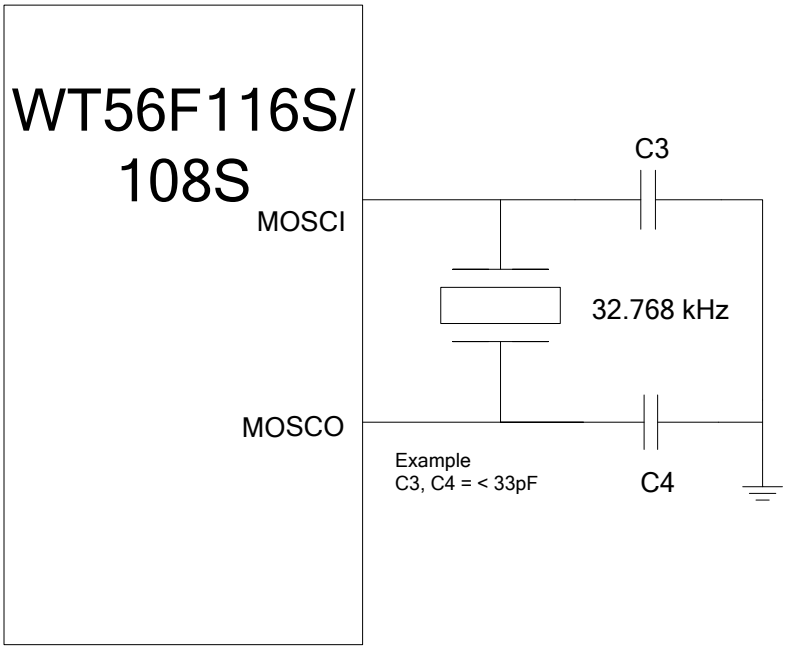
Crystal Oscillator	C1, C2 = 0pF ~ 68pF
Ceramic Resonator	C1, C2 = 0pF ~ 68pF

* The example load capactor value(C1,C2,C3,C4) is common value but may not be appropriate for some crystal or ceramic resonator.

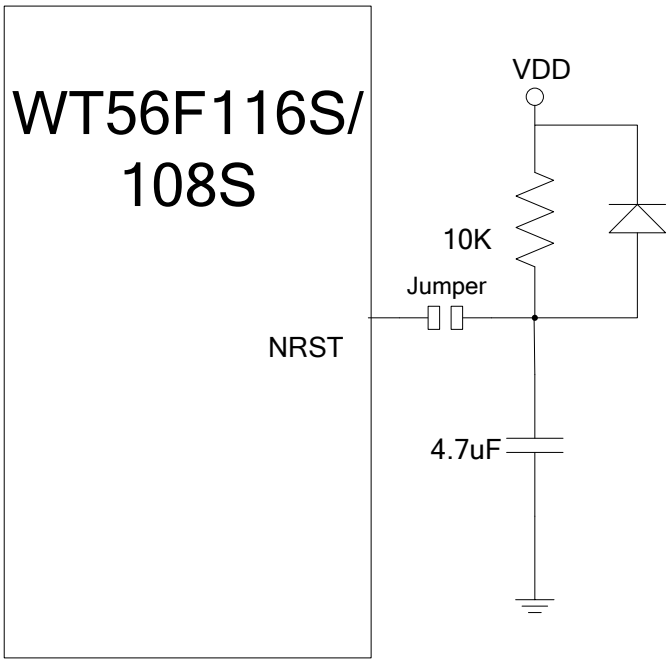


Note: WT56F116S/108S has built-in internal RC oscillators, thus external crystal oscillators are not essential. If for more precise application, external crystal oscillator is available for use.

8.2.2 External 32.768 kHz Crystal Oscillator

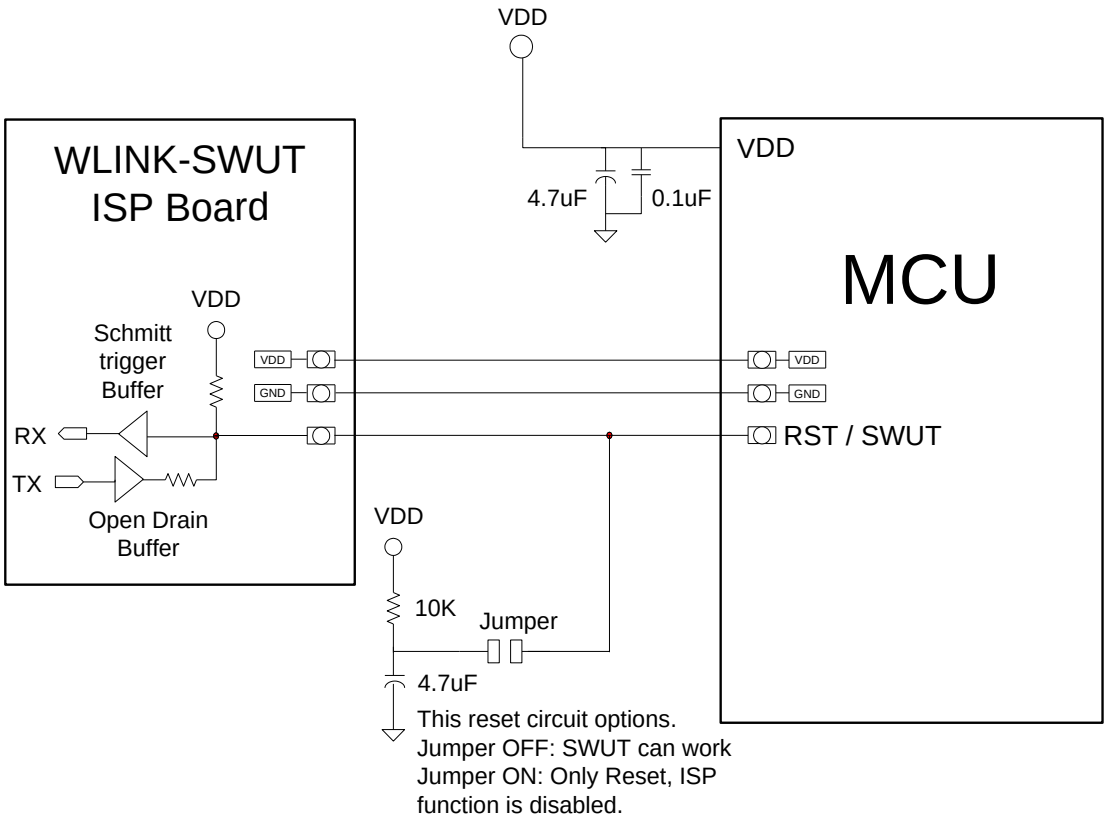


8.3 RESET Circuit

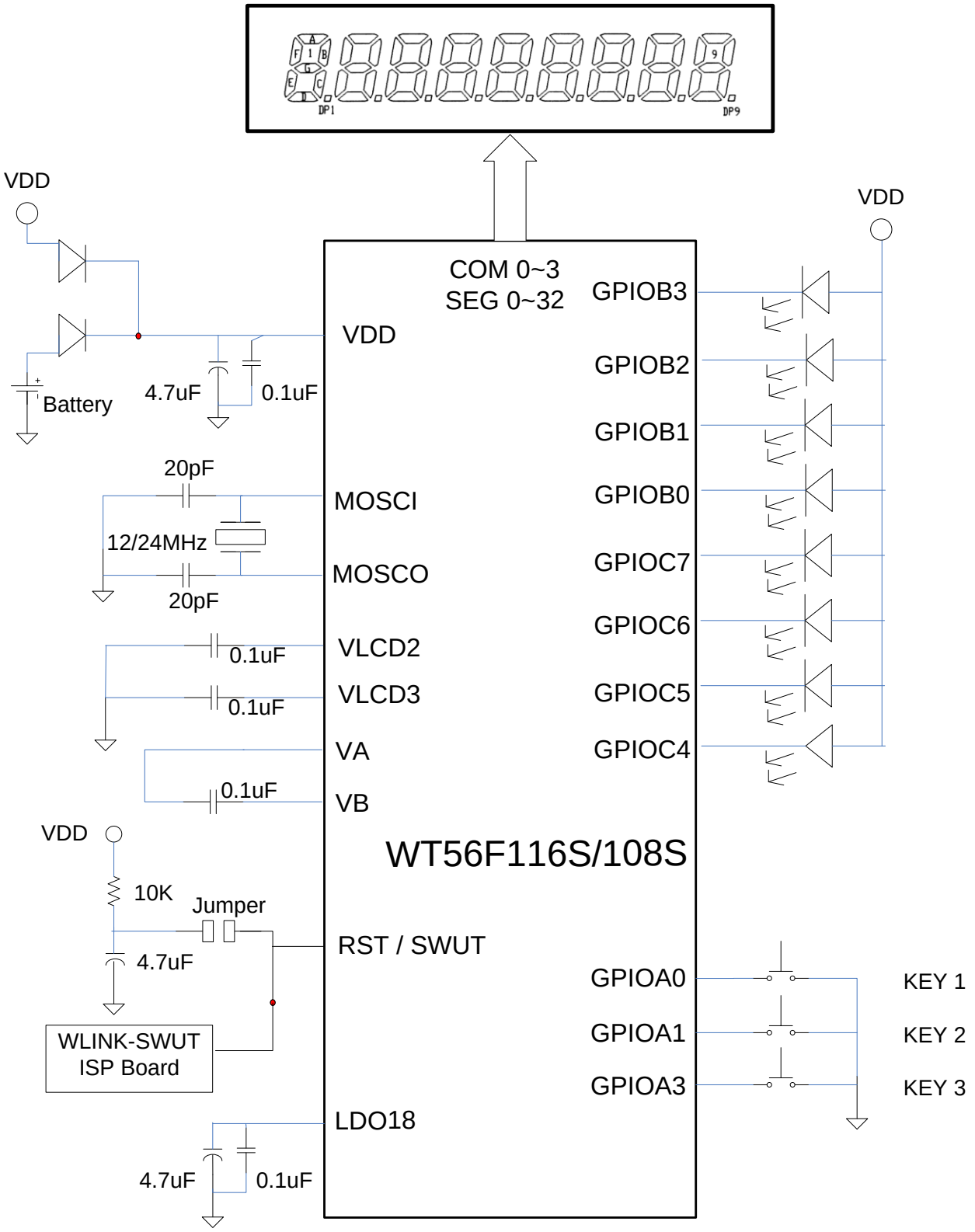


Note: Reset Circuit will affect programming process, and it requires adding Jumper for isolation.

8.4 Standard Circuit



8.5 Development board circuits (4COM LCD)



9. Product Naming Rule

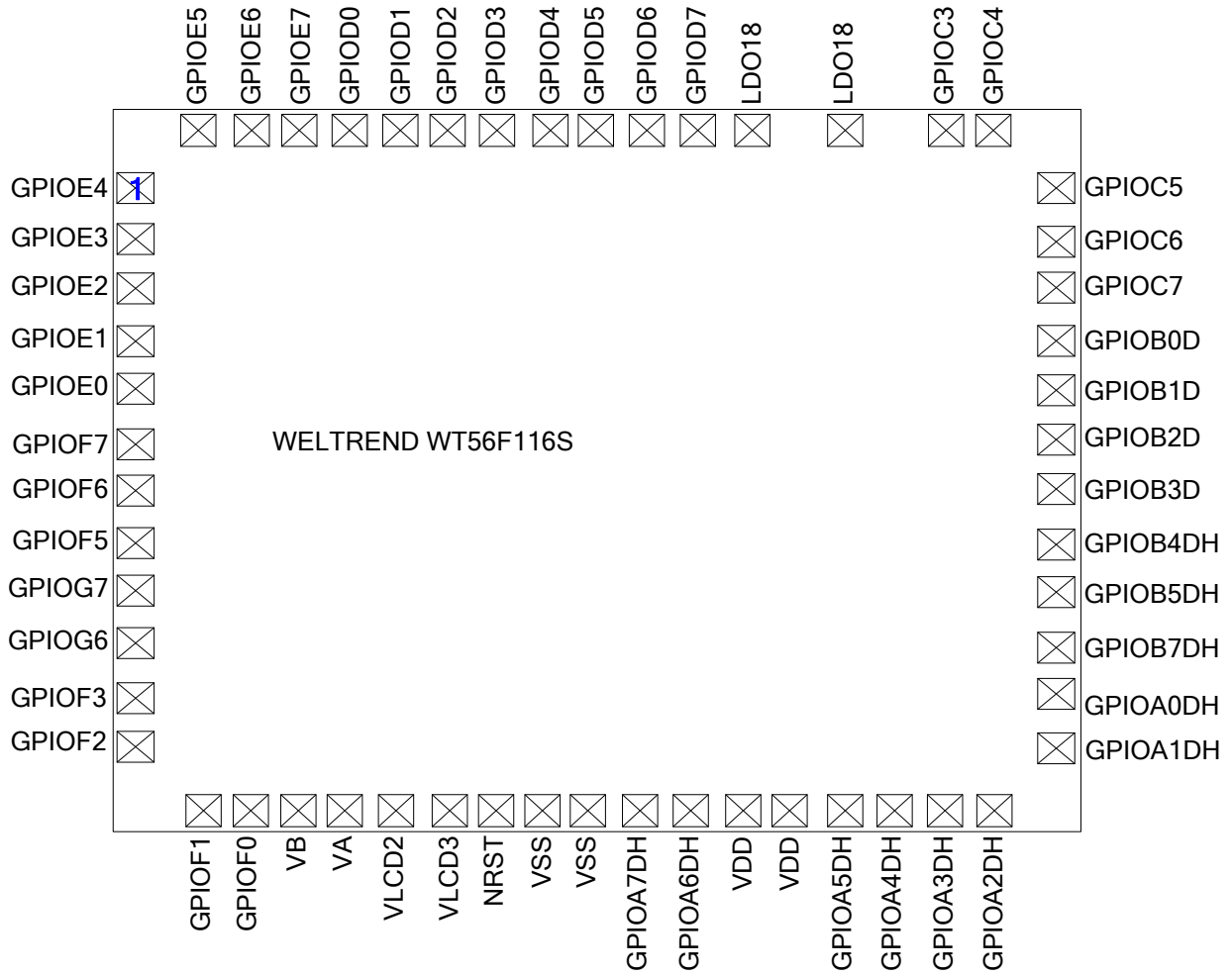
WT	Consumption market	LCD function	Seed code (Family)	Flash Size (K Bytes)		Remarks
WT	5	1F	1	0	4	5: MCU/DSP embedded, used in general-purpose or consumption market related product. 1F: Flash type 8-bit MCU without LCD function 6F: Flash type 8-bit MCU with LCD function
			1	0	4 S	
			1	0	8	
			1	0	8 S	
			1	1	6	
			5	1	6	
WT	5	6F	1	0	8	
			1	0	8 S	
			1	1	6 S	
			2	1	6	
			2	3	2	
			2	4	8	

10. Ordering Information

Package Type	Package Outline	Part Number
64-pin LQFP	7mm x 7mm	WT56F116S-RG64AWT
48-pin LQFP	7mm x 7mm	WT56F116S-RG48AWT
SOP28	300 mil	WT56F116S-SG28AWT
SSOP20	150 mil	WT56F116S-OG20AWT
Wafer form or Chip form	-	WT56F116SHXXXWT

Package Type	Package Outline	Part Number
64-pin LQFP	7mm x 7mm	WT56F108S-RG64AWT
48-pin LQFP	7mm x 7mm	WT56F108S-RG48AWT
SOP28	300 mil	WT56F108S-SG28AWT
SSOP20	150 mil	WT56F108S-OG20AWT
Wafer form or Chip form	-	WT56F108SHXXXWT

11. Pad Diagram & Location Table



PAD Location

No	Name	X	Y	No	Name	X	Y
1*	GPIOE4	46.26	1351.29	29	GPIOA2DH	1884.74	46.26
2*	GPIOE3	46.26	1244.49	30*	GPIOA1DH	2013.74	175.26
3*	GPIOE2	46.26	1137.69	31*	GPIOA0DH	2013.74	282.26
4*	GPIOE1	46.26	1030.89	32*	GPIOB7DH	2013.74	389.26
5*	GPIOE0	46.26	924.09	33*	GPIOB5DH	2013.74	496.26
6*	GPIOF7	46.26	817.26	34*	GPIOB4DH	2013.74	603.26
7*	GPIOF6	46.26	710.26	35*	GPIOB3D	2013.74	710.26
8*	GPIOF5	46.26	603.26	36*	GPIOB2D	2013.74	817.26
9*	GPIOG7	46.26	496.26	37*	GPIOB1D	2013.74	924.26
10*	GPIOG6	46.26	389.26	38*	GPIOB0D	2013.74	1030.94
11*	GPIOF3	46.26	282.26	39*	GPIOC7	2013.74	1137.74
12*	GPIOF2	46.26	175.26	40*	GPIOC6	2013.74	1244.54
13	GPIOF1	175.26	46.26	41*	GPIOC5	2013.74	1351.34
14	GPIOF0	282.26	46.26	42	GPIOC4	1884.74	1479.74
15	VB	389.26	46.26	43	GPIOC3	1777.74	1479.74
16	VA	496.26	46.26	44	LDO18	1565.99	1479.74
17	VLCD2	603.26	46.26	45	LDO18	1362.74	1479.74
18	VLCD3	710.26	46.26	46	GPIOD7	1245.26	1479.74
19	NRST	818.26	46.26	47	GPIOD6	1138.26	1479.74
20	VSS	917.76	46.26	48	GPIOD5	1031.26	1479.74
21	VSS	1016.26	46.26	49	GPIOD4	924.26	1479.74
22	GPIOA7DH	1123.26	46.26	50	GPIOD3	817.26	1479.74
23	GPIOA6DH	1230.26	46.26	51	GPIOD2	710.26	1479.74
24	VDD	1344.76	46.26	52	GPIOD1	603.26	1479.74
25	VDD	1443.26	46.26	53	GPIOD0	496.26	1479.74
26	GPIOA5DH	1563.74	46.26	54	GPIOE7	389.26	1479.74
27	GPIOA4DH	1670.74	46.26	55	GPIOE6	282.26	1479.74
28	GPIOA3DH	1777.74	46.26	56	GPIOE5	175.26	1479.74

Notes:

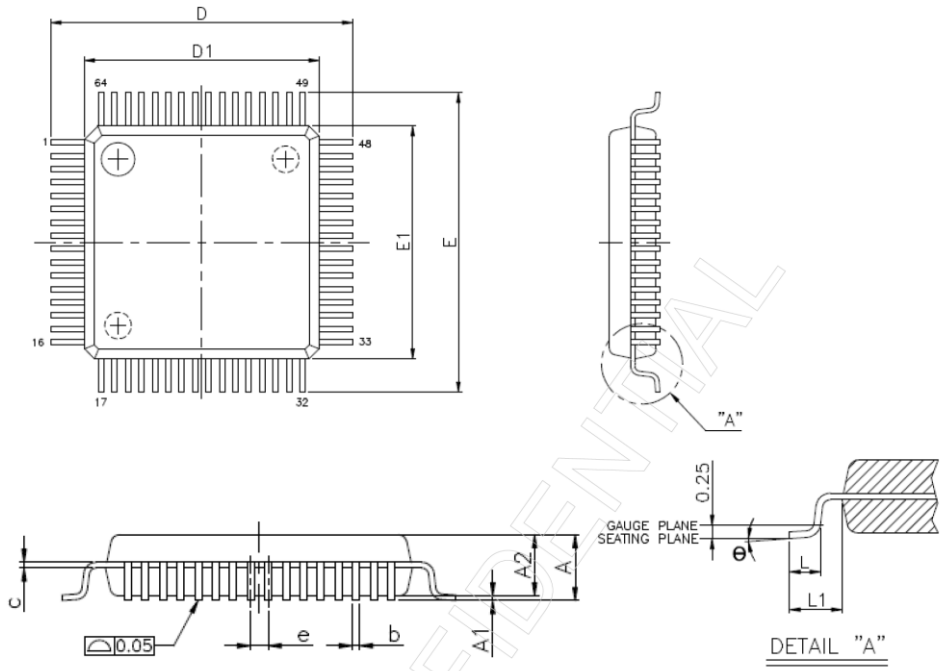
1. *The origin of pad location shown here is at lower-left corner of die.*
2. *PAD Window, use circuit under PAD(CUP)*
   (a) *A type: 63um x 66um*
   (b) *B type: 66 um x 63um (*)*
3. *To stabilize the supply voltages, please connect 0.1uF and 4.7uF bypass capacitors between VDD and VSS.*
4. *To stabilize the supply voltages, please connect 0.1uF and 4.7uF bypass capacitors between LDO18 and VSS.*
5. *All VDD pin need connect together. (No: 24, 25)*
6. *All VSS pin need connect together. (No: 20, 21)*
7. *All LDO18 pin need connect together. (No: 44, 45)*

12. Package Dimension

12.1 64-Pin LQFP

1. Package Outline

Low-Profile Quad Flat Package **LQFP-64 PIN**



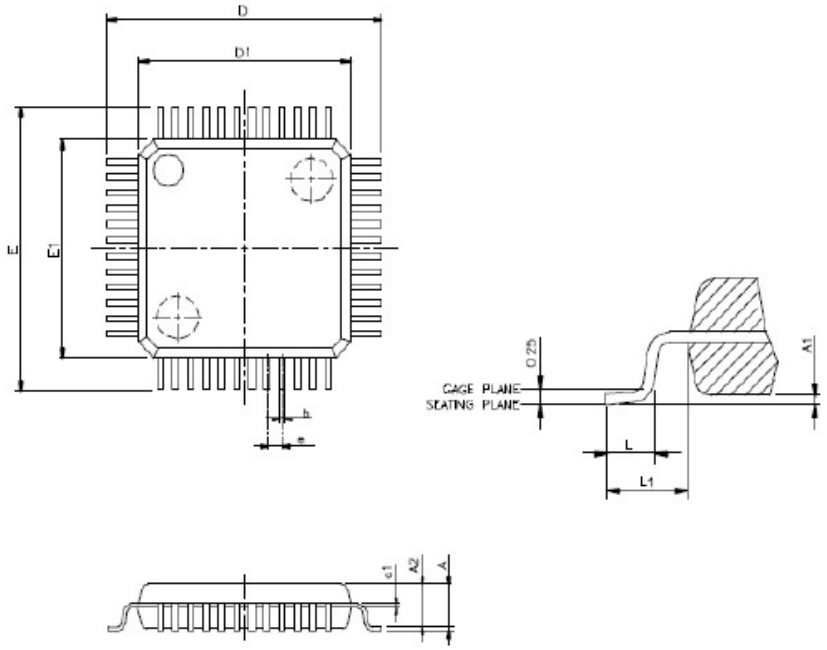
SYMBOLS	MIN	NOR	MAX
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	-	0.20
D		9.00 BSC	
D1		7.00 BSC	
e		0.40 BSC	
E		9.00 BSC	
E1		7.00 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ°	0	3.5	7

UNIT: mm

NOTES:
1. JEDEC outline : MS-026 BBD
2. Dimensions "D1" and "E1" do not include mold protrusion. Allowable protrusion is 0.25mm per side. "D1" and "E1" are maximum plastic body size dimensions including mold mismatch.
3. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum "b" dimension by more than 0.08mm.

PREPARE	Cynthia	DATE: 2012/7/27
CHECK	Lawrence	DATE: 2012/7/27
APPROVE	Eric	DATE: 2012/7/27

12.2 48-Pin LQFP



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

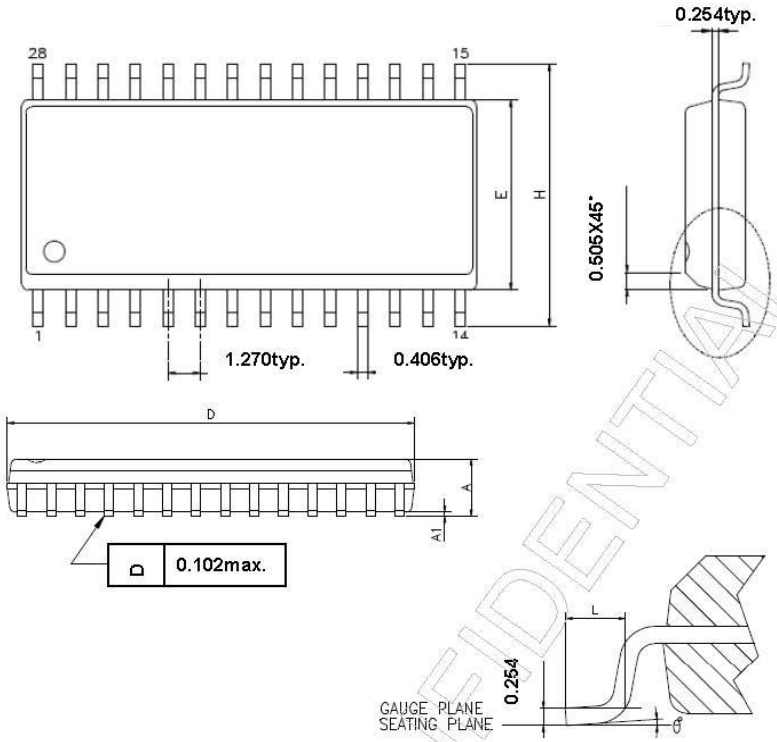
SYMBOLS	MIN.	MAX.
A	--	1.6
A1	0.05	0 15
A2	1.35	1.45
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
E	9.00 BSC	
E1	7.00 BSC	
e	0.5 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	

NOTES:
1. JEDEC OUTLINE: MS-026 BBC
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

12.3 28-Pin SOP

Small Outline Package

300MIL/SOP-28 PIN



SYMBOLS	MIN	NOR	MAX
A	-	-	2.642
A1	0.102	-	-
D	17.704	18.237	18.390
E	7.391	7.493	7.595
H	10.008	10.312	10.643
L	0.406	0.889	1.270
θ°	0	4	8

UNIT: mm

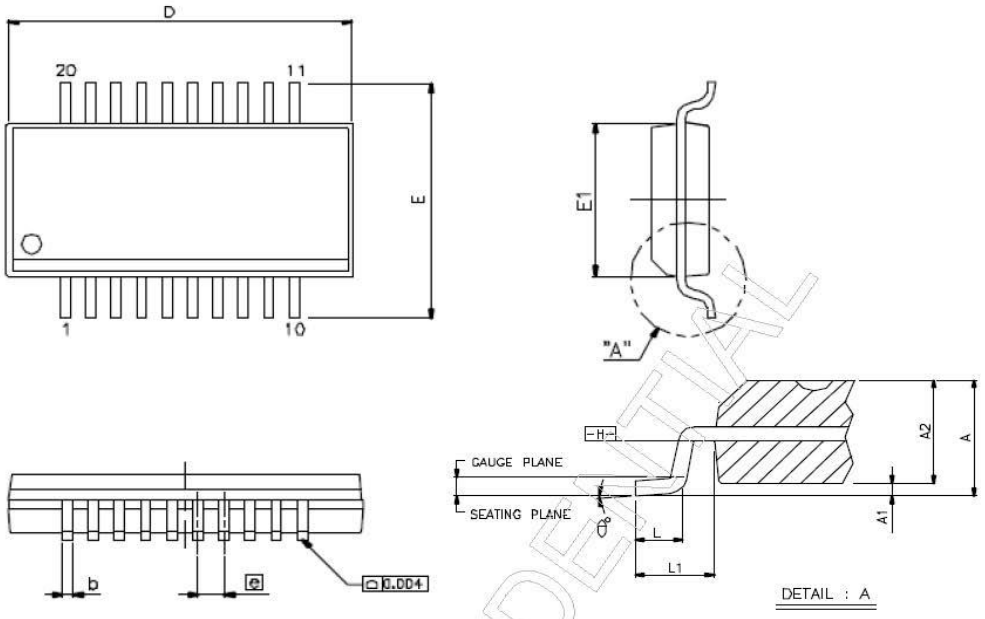
NOTES:
1. JEDEC outline : MO-119 AB
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions and gate burrs shall not exceed 0.15mm per side.
3. Dimension "E" does not include inter-lead flash, or protrusions. Inter-lead flash and protrusions shall not exceed 0.25mm per side.

PREPARE	Cynthia	DATE: 2013/1/16
CHECK	Lawrence	DATE: 2013/1/16
APPROVE	Eric	DATE: 2013/1/16

12.4 20-Pin SSOP

Shrink Small Outline Package

150MIL/SSOP-20PIN



SYMBOLS	MIN	NOR	MAX
A	1.346	1.626	1.753
A1	0102	0.152	0.254
A2	-	-	1.499
b	0.203	-	0.305
C	0.178	-	0.254
D	8.560	8.661	8.738
E	5.791	5.994	6.198
E1	3.810	3.912	3.988
e	0.635 BSC		
L	0.406	0.635	1.270
L1	1.041 BSC		
θ°	0	-	8

UNIT: mm

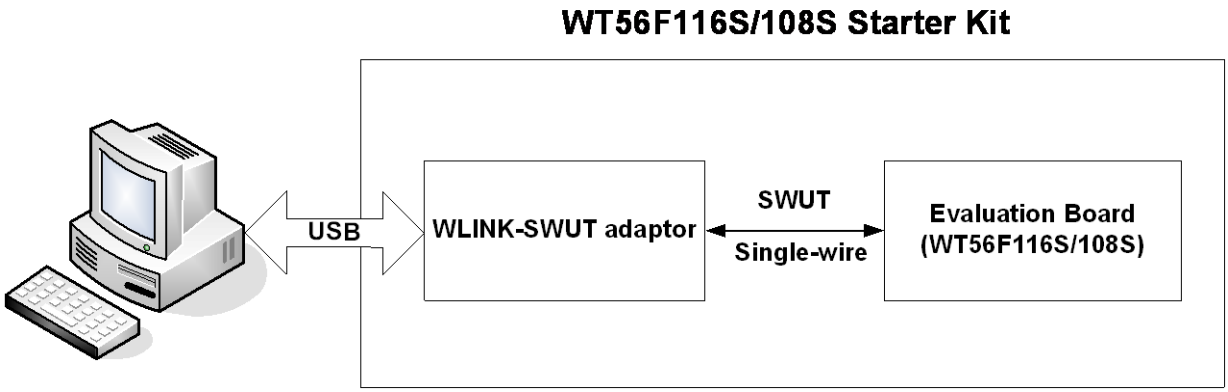
NOTES:
1. JEDEC outline : MO-137AD
2. Dimension "D" does not include mold protrusion or gate burrs. Mold protrusions and gate burrs shall not exceed 0.152mm per side. Dimension "E1" does not include inter-lead mold protrusions. Inter-lead mold protrusion shall not exceed 0.254mm per side.
3. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.102mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.051mm at least.

PREPARE	Cynthia	DATE: 2012/7/26
CHECK	Lawrence	DATE: 2012/7/26
APPROVE	Eric	DATE: 2012/7/26

13. Development Tools

WT56F116S/108S can work together with Keil C51 development environment. WLINK adaptor can link PC and WT56F116S/108S evaluation board via ICE/ISP driver, and the debugger tools, demo board application software can perform In-Circuit Emulator (ICE) and In-system Programming (ISP) in Windows 98/2000/XP/Win7.

The development kits are illustrated in the figure below:



Development Tools List:

Please go to Weltrend's website http://www.weltrend.com.tw/ for more information.

Product Information	**General Purpose IC**	ADC Type MCU	WT51F104 Product Spec
			WT51F116/WT51F108 Product Spec
		ADC+LCD Type MCU	WT56F216 Product Spec
			WT56F116S/108S Product Spec
			WT56F248/WT56F232 Product Spec
Technical Support	**Supporting Tools/ General Purpose IC**	ICE/ISP	**WA001** WLINK-SWUT Adapter
		Mass Production Programming	**WA007 WLINK-SWUT-M4S**
		Mass Production Programming Daughter Board	**WS001** WLINK-SWUT-M4S Daughter Board Support WT56F216/WT56F232/WT56F248 MCU RG44AWT LQFP 44 PKG
			WS003 WLINK-SWUT-M4S Daughter Board Support WT56F216 MCU SG28AWT SOP28 PKG
			WS004 WLINK-SWUT-M4S Daughter Board Support WT51F104/WT51F116/WT51F108 MCU OG20AWT SSOP20 PKG
			WS005 WLINK-SWUT-M4S Daughter Board Support WT51F104 MCU SG140WT SOP14 PKG SG080WT SOP8 PKG
			WS006 WLINK-SWUT-M4S Daughter Board Support WT51F104 MCU MG10AWT MSOP10 PKG
			WS007 WLINK-SWUT-M4S Daughter Board Support WT56F108/WT56F116S MCU RG64AWT LQFP64 PKG
			WS009 WLINK-SWUT-M4S Daughter Board Support WT51F116/WT51F108 MCU UG32AWT QFN32 PKG
			WS010 WLINK-SWUT-M4S Daughter Board Support WT51F116/WT51F108 MCU MG10BWT MSOP10 PKG
			WS011 WLINK-SWUT-M4S Daughter Board Support WT56F248/WT56F232 MCU RG64AWT LQFP64 PKG
			WS012 WLINK-SWUT-M4S Daughter Board Support WT56F248/WT56F232 MCU UG32AWT QFN32 PKG
			WS013 WLINK-SWUT-M4S Daughter Board Support WT56F108/WT56F116S MCU RG44AWT LQFP 44 PKG
			WS014 WLINK-SWUT-M4S Daughter Board Support WT56F108/WT56F116S MCU SG28AWT SOP28 PKG

Technical Support	**Supporting Tools/ General Purpose IC**	Evaluation Board	**WB000** WT56F216 EV Board
			WB001 WT51F104 EV Board
			WB005 WT56F216 Starter Kit Board
			WB006 WT51F104 Starter Kit Board
			WB007 WT56F108/WT56F116S Starter Kit Board
			WB008 WT51F116/WT51F108 Starter Kit Board
			WB010 WT56F248/WT56F232 Starter Kit Board
		Starter Kit	**WK000** WT56F216 Starter Kit
			WK001 WT51F104 Starter Kit
			WK004 WT56F108/WT56F116S Starter Kit
			WK005 WT51F116/WT51F108 Starter Kit
			WK007 WT56F248/WT56F232 Starter Kit
	Technical Data/ General Purpose IC	WLINK Adapter Operation Manual	**Doc2** WLINK-SWUT Adapter Installation Manual
		Mass Production Programming Operation Manual	**Doc26** WLINK-SWUT-M4S Operation Manual
		ICE/ISP Operation Manual	**Doc6** WLINK ICE Operation Manual (uVision IDE Version)
			Doc8 WLINK-SWUT ISP Operation Manual (for Alone Programmer)
		Evaluation Board Operation Manual	**Doc12** WT56F216 EV Board Operation Manual
			Doc13 WT51F104 EV Board Operation Manual
			Doc21 WT56F216 Starter Kit Quick Start Guide
			Doc22 WT51F104 Starter Kit Quick Start Guide
			Doc23 WT56F216 Starter Kit Operation Manual
			Doc24 WT51F104 Starter Kit Operation Manual
			Doc27 WT56F116S/108S Starter Kit Operation Manual
			Doc28 WT51F116/WT51F108 Starter Kit Operation Manual
			Doc30 WT56F248/WT56F232 Starter Kit Operation Manual
		Mass Production ISP and Supplier Contact Information	**Doc20** Mass Production ISP Supplier

Technical Support	**Software Download/ General Purpose IC**	WLINK Adapter Driver	**SW2** WLINK-SWUT Adapter Driver
		Mass Production Programming Driver	**SW2** WLINK-SWUT Adapter Driver
		ICE Driver/ISP Program	**SW6** WLINK-SWUT ICE Driver (for uVision IDE)
			SW8 WLINK-SWUT ISP Driver (for uVision IDE)
			SW9 WLINK-SWUT ISP Program (for Alone Programmer)
			SW17 Auto-install WLINK-SWUT ICE & ISP Driver (for uVision IDE) WLINK-SWUT ISP Driver (for uVision IDE)
		Example Program	**SW13** WT56F216 EV Board Example Program
			SW14 WT51F104 EV Board Example Program
			SW18 WT56F216 Starter Kit Board Example Program
			SW19 WT51F104 Starter Kit Board Example Program
			SW21 WT56F108/WT56F116S Starter Kit Board Example Program
			SW22 WT51F116/WT51F108 Starter Kit Board Example Program
			SW25 WT56F248/WT56F232 Starter Kit Board Example Program

14. Revision History

Version	History	Date
1.0	Initial issue	May 2017